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Absorber and Window Study – CdSexTe1-x/CdTe Thin Film Solar Cells

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Absorber and Window Study – $CdSe_xTe_{1-x}$/CdTe Thin Film Solar Cells

by

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of the requirements for the degree of
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ABSTRACT

CdTe an II-VI semiconductor has been a leading thin film photovoltaic material due to its near ideal bandgap and high absorption coefficient [1]. The typical thin film CdTe solar cells have been of the superstrate configuration with CdS (E_g-2.42eV) as the n-type heterojunction partner. Due to the relatively narrow bandgap of CdS, a wider bandgap n-type window layer has recently emerged as a promising substitute: alloys of $Mg_yZn_{1-y}O$ have been successfully used as the emitter or window layer. The benefits in the usage of $Mg_yZn_{1-y}O$ (MZO) are its tunable bandgap and wide optical spectrum on optoelectronic devices. Due to an increasing bandgap of the window layer, the carrier collection can be improved in the short wavelength range (<500 nm). In addition alloys of $CdSe_xTe_{1-x}$ (CST) have also been used in the absorber layer (i.e., CST/CdTe) for the fabrication of CdTe devices to improve the carrier collection and lifetime [2]. The lower bandgap of the CST alloy can lead to higher short-circuit current (J_{SC}), but it can also result in lower open circuit voltage (V_{OC}). Another critical aspect of the CdTe solar cell is the use of copper as a p-type dopant, which is typically incorporated in the cell during the fabrication of the back contact. The most challenging issue related to further advancing the CdTe solar cell efficiency is the relatively low level of p-type doping, which limits the V_{OC}. Efforts to dope CdTe with group V dopants are yet to produce the desired results.

ZnO has been used as an effective high resistivity transparent. When CdTe is deposited directly on sputtered ZnO, V_{OC} of typically 500-600 mV is produced. Band alignment measurements indicate that a negative conduction band offset with CdS exists; alloying with MgO to produce $Mg_yZn_{1-y}O$ with a composition of y = 0.15 can produce a flat conduction band

alignment with CdS. This material has an additional benefit for improving the energy bandgap of the MZO for better UV light transmission in the short wavelengths. By changing the magnesium content from y = 0 to 0.30 allowed researchers to make the tunable conduction band offset from a *"cliff"* to a *"spike,"* with both increased open-circuit voltage and fill factor as increasing magnesium compositions [3] — the bandgap gains as expected with increased magnesium composition. The large compositions (y > 0.30) of $Mg_yZn_{1-y}O$ cause the enormous spike result in S-kink in the IV measurement so that the FF decreases. Besides, due to the instability of MZO material, the fabrication process has to proceed carefully.

The properties of CST films and cells were investigated as a function of Se composition (x), substrate temperature (T_{SUB}), and ambient used during the CSS deposition. The higher ratio of Se in CST alloy causes the smaller grain structures and lower bandgap, which profoundly detrimental to the device performance (V_{OC}). However, the CST can be deposited in various substrate temperatures and different inert ambient gas to improve the grain structure by utilizing the especial Close Space Sublimation (CSS) deposition system. Therefore, despite the fact that the CST (25% Se) has the optical bandgap (1.37eV), the improvement of grain structure can slightly increase the doping concentration and decrease the grain boundary (GBs) due to increased alloys grain size 3X larger, which is contributed to improving the V_{OC} [4]. The study of higher ratio Se of CST alloy is significant to achieve the high efficiency polycrystalline CST/CdTe photovoltaic devices.

The effect of Cu doping back contact in $CdSe_xTe_{1-x}$ (CST)/CdTe solar cells with varying amounts of Se (x) has been investigated. The Cu-based back contact was annealed at different thermal temperatures in order to vary the amount of Cu in-diffusion. Net p-type doping was found to increase as the back-contact annealing temperature increased. All cells exhibited a decrease in

V_{OC} with increased annealing temperature (i.e., higher Cu concertation), presumably due to a degradation of the lifetime with increased amounts of Cu [5]. However, cells with the highest Se composition appeared to exhibit a higher degree of tolerance to the amount of Cu – i.e., they exhibited a smaller loss in V_{OC} with the increased amount of Cu.

Extrinsic p-type doping of CdSeTe can be fabricated using two different experimental processes. Firstly, by using group I elements such as, Cu to substitute Cd, which is promising during the back contact process. Secondly, using group V (P, As, Sb) elements to substitute Te, and this is suitable for Cd-rich of intrinsic CdTe. Intrinsic CST alloy has lower hole density concentration as higher Se composition with limitation of the V_{OC}. Thus, in order to increase the p-type net doping up to 10^{16} cm^{-3} the extrinsic P or As doping have been widely investigated recently. The research studies show the CST/CdTe devices lead to improve V_{OC} up to 850 mV with higher hole density in higher Se compositions of As doped CST alloys. Nevertheless, the group V doped CdTe still cause the formation of compensating defects limits the upper boundary of dupability on the CdTe thin film solar cells. Even if a high hole density concentration is achieved for intrinsically-doped p-type CST/CdTe, it is believed the poor carrier lifetime in the CdTe side would still limit the V_{OC}.

CHAPTER 1

INTRODUCTION

Natural gas and non-renewable energy provide around 79% of the world's electrical power sources in North America and 90% of the world's total energy demands [6]. As the worldwide market for energy is higher than the consumption of supplies, the expense of supplying electricity becomes more expensive, and it is anticipated that by 2030 the cost of non-renewable generated electricity will exceed that of renewable sources. Another major concern is global warming (greenhouse issue), and climate changes are relatively associated with the use of those fossil fuels (coal, oil, and natural gas, etc,) as reported at the G20 summit [7]. However, it is critical to change to an energy power which is clean, efficient, and sustainable. The common renewable energy sources like wind, solar, marine, and small-scale hydropower currently provide around 2% of the world's electrical energy consumption. The statistics of the energy demands and use (LCOE analysis) for the present and the future are shown in Figure 1 [8]. Therefore, the most significant renewable source of energy is solar energy, which is abundant. The sun is a crucial source of inexhaustible free energy for our planet Earth. Currently, new technologies are being employed to generate electricity from harvested solar energy. As the sun's radiation penetrates towards the earth's surface, the various spectrum of sunlight is continuously absorbed and re-emitted at very low temperatures, so that by the time they reach the surface, it is visible light. Approx. 97% of the total sunlight energy released by the sun in the outer space generates is between the wavelengths of 0.25 to 3.0μm. The development of PV technologies is pivotal for efficiently converting solar radiation into electricity.

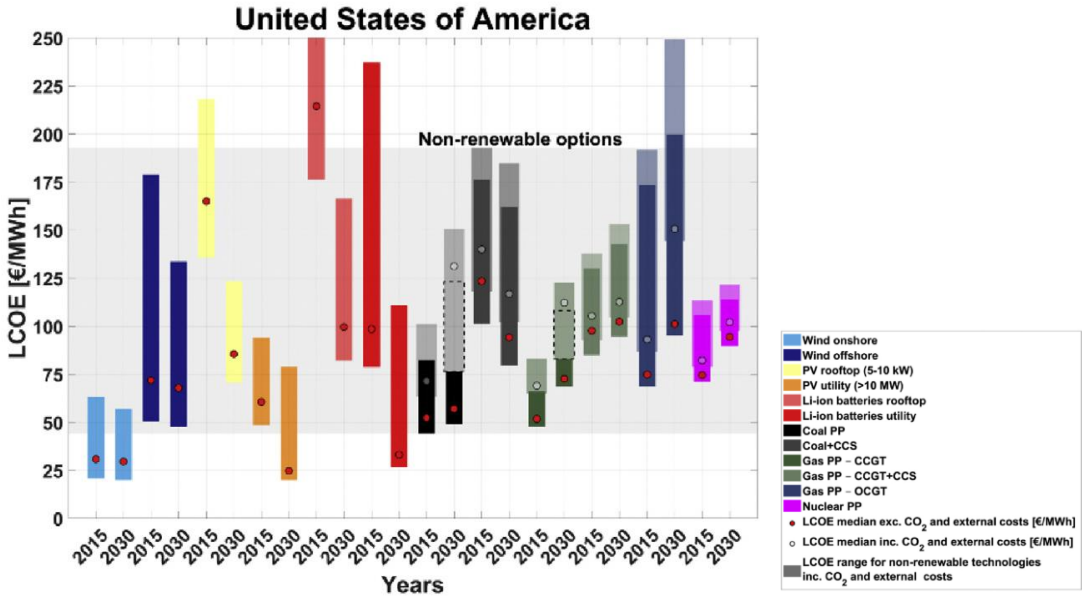


Figure 1 Results of LCOE calculations for the United States in 2015 and 2030 [8].

1.1 PV Technologies

Solar energy is clean and abundant with zero carbon emissions and is expected to be available for millions of years. A solar cell converts solar energy directly into electricity through the photovoltaic effect. Photovoltaics is a critical energy technology which has a small impact on the environment as it generates electricity from light, produces no air pollution or hazardous waste. It does not require fuels to be transported or combusted. Regarding the protection of the environment, my work contributes to the advancement of low cost and high efficiency CdTe based thin film solar cells which can be manufactured at lower costs in comparison to mainstream silicon wafer-based solar cells.

1.1.1 Wafer Based PV

Wafer based PV commonly utilizes silicon (Si), germanium (Ge), and gallium arsenide (GaAs) as substrates to manufacture the solar cells devices, which are shown in Figure 2. In the commercial market, three different types of wafer based PV technologies are discussed below:

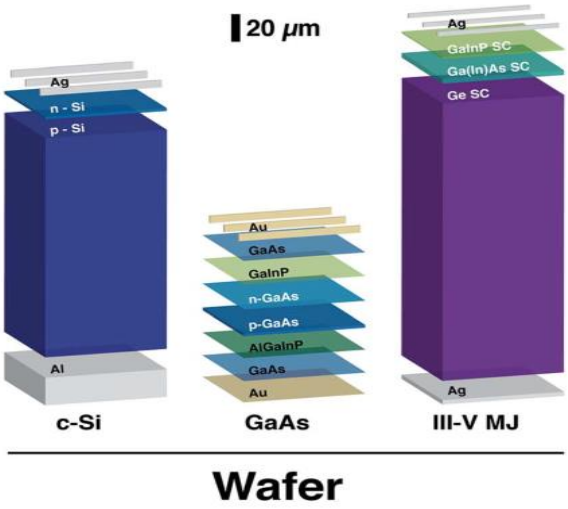


Figure 2 The PV technologies of wafer based solar cells [6].

1.1.1.1 Crystalline Silicon

Silicon based PV is the most common PV technology. It is based on single crystalline silicon (c-Si), or multi-crystalline silicon (multi-Si) consisting of small crystals. C-Si and multi-Si cells are assembled into solar panels or modules as part of photovoltaic devices to generate solar power. The electronic properties of crystalline silicon are well understood and controlled through years of development for the manufacture of microchips (i.e., IC technology). It can be produced with very low impurity levels. Production of electronic silicon includes a chemical purification to produce hyperpure polysilicon followed by a recrystallization fabrication process to form monocrystalline silicon in the form of cylindrical boules. The cylindrical boules are then cut into wafers for the next fabrication process as the semiconductor material. Solar cells devices are fabricated by using crystalline silicon are often called conventional, traditional, or first-generation solar cells, as they were first developed in the 1950s and remained the most common type up to the present time [9][10]. Compared to thin film solar cells (like CdTe which is the main topic of this dissertation) c-Si cells are manufactured from 150 – 200 μm thickness of solar wafers due to the low optical absorption coefficient for Si material.

1.1.1.2 GaAs Solar Cells

III-V solar cells, e.g., utilizing gallium arsenide (GaAs) as substrates. GaAs (similar to CdTe) has a high optical absorption coefficient, and therefore GaAs solar cells can be fabricated to small thicknesses. Their efficiency is the highest of any single junction solar cell with 28.9% (measured under the AM1.5G spectrum (approx. 1000 W/m^2) at 25 degrees Celsius) [11, 12]. The advantage of this high solar cell efficiency, however, is compensated by the expensive costs compared to traditional silicon solar technologies and thin film solar cells, which have slowed down their development for terrestrial applications. Many approaches have been developed for cost down on GaAs solar cells and still maintaining their high conversion efficiency. Amongst the various type of developments, two are worthy of further development, specifically: a) reusable GaAs substrate [13], or b) decreased the thickness of the GaAs as absorber layer [14, 15] and therefore lower the materials costs.

1.1.1.3 III-V Multi-Junction Cells

Multi-junction cells consist of multiple Group III-V thin film materials typically grown using metalorganic vapor phase epitaxy(MOVPE) [16]. Each Group III-V compound has a tunable bandgap energy to allow it to absorb a different portion of the solar spectrum. Multi-junction solar cells are the most expensive PV technology, but their high efficiency and relatively low weight make them the most suitable option for satellites and similar space applications. In terrestrial applications, they have been utilized in concentrator photovoltaics (CPV), where low-cost lenses and curved mirrors are used to concentrate sunlight onto small area highly efficient multi-junction solar cells. Nowadays, typical triple-junction solar cells consist of monolithic Group III-V materials such as gallium indium phosphide (GaInP), gallium arsenide (GaAs), and germanium (Ge) as p-n junctions, offer high efficiencies and market demand appears to be increasing, despite

the high cost [17][18]. GaAs based multijunction devices are the most efficient PV technologies to date. The most recent record, triple-junction metamorphic cells reached a record high of 44% [19].

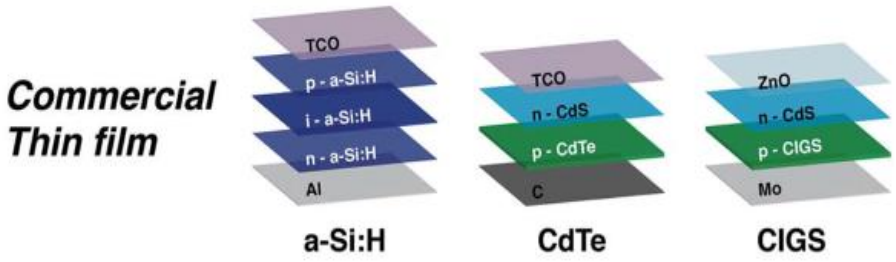


Figure 3 The most common commercial thin film solar cell in the industrial market [6].

1.1.2 Commercial Thin Film Solar Cells

Although silicon-based, (C-Si and multi-Si) solar modules still dominate the photovoltaics' (PV) market, emerging thin film technologies based on CdTe and CIGS have been successfully commercialized and offer a lower cost alternative. The advantages of semiconductor properties include higher absorption coefficients and direct bandgap, which are applied in the thin film solar cells. The benefits allow the thickness of the absorber layer decreases from a hundred microns (μm) to only a few microns. Therefore, the actual raw materials have been used for fabricating the thin film solar cells that it is believed to be lower than crystalline Si technology. Today's most common thin film solar cells are including amorphous Si, cadmium telluride (CdTe), and copper indium gallium diselenide (CIGS) as shown in Figure 3.

1.1.2.1 Amorphous Si

Amorphous silicon (a-Si) is the non-crystalline structure of silicon. It is used for solar cells and thin film transistors in optoelectronic devices. Due to the low deposition temperatures associated with this material, it can be deposited onto different types of flexible substrates, such

as glass, metal, and plastic. Amorphous silicon (a-Si) solar cells are typical of lower efficiency and suffer from an inherent instability mechanism, but the technology is one of the most environmentally friendly PV technologies since the productions do not use any toxic heavy metals such as cadmium or lead [20]. As a second-generation and commercial thin-film solar cell technology, amorphous silicon was once anticipated to become a significant contributor in the fast-growing worldwide photovoltaic market in the high volume manufacturing, but has since lost its significance due to intense competition from traditional crystalline silicon solar cell and other thin film PV technologies, like CdTe and CIGS [21].

1.1.2.2 CdTe Thin Film Solar Cells

The theoretical efficiency of CdTe is very promising among the semiconductors materials available today for a single-junction device architecture due to the bandgap of CdTe (1.45 eV). CdTe PV technology has manufactured and installed with the global capacity of >20 GW. Due to its thermal and chemical stability are recent advances in efficiency compared, it is expected to continue to be a significant part of the PV technology mix. The US Department of Energy (DOE) anticipates that CdTe thin film solar cell is well-matched for utility-scale applications and high volume manufacturing to decrease the cost-effectiveness of electricity per watt by 2030 [22].

1.1.2.3 Copper Indium Gallium Diselenide (CIGS)

Similar to CdTe based solar cell, cadmium indium gallium diselenide (CIGS) devices also have a very high absorption coefficient and high efficiency. In addition, the cost of CIGS solar devices has not matched that of CdTe, and production volumes remain low. The power conversion efficiency of CIGS has already surpassed over 22%. CIGS thin film solar cell is perfectly favorable for building integrated PV applications because it can be manufactured on flexible and lightweight substrates.

1.1.3 Emerging Thin Film PV

Emerging PV technologies also known as the third generation photovoltaic cells are still relatively immature and at the early stages of research and development. Figure 4. shows the different categories of new advanced PV technologies that have been developing recently.

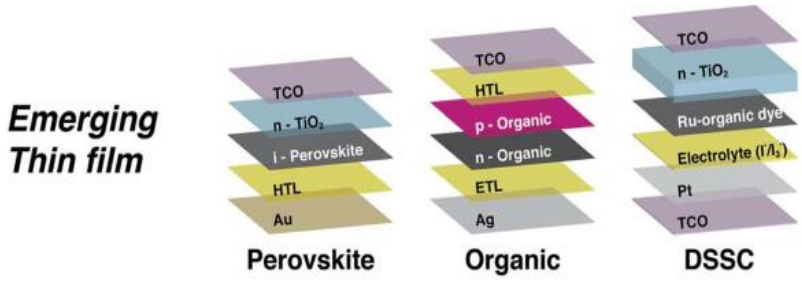


Figure 4 Ongoing development PV technologies in the emerging thin film solar cells [6].

1.1.3.1 Dye-sensitized Solar Cells

Dye-sensitized solar cells (DSCs) are thin film cells. They are named dye-sensitized solar cells (DSSC) or Grätzel cells called after the Swiss chemist Michael Grätzel, who was first to invent this new type of PV technology [23]. The fabrication process of DSCs is simple, generally low cost, and utilize environmentally safe materials, which have a competitive efficiency (about 10-14 %) even the sunlight is performed with low flux [24]. Nevertheless, one of the disadvantages is the temperature sensitivity of the liquid electrolyte. Consequently, the most recent research is still trying to enhance the electrolyte's performance and cell for stability or finding the new type of organic materials or devices.

1.1.3.2 Organic Solar Cells

Organic solar cells can be defined by the experimental process of solar cells, the property of the materials, and the device layout. The two main fabrication process for productions can be categorized as either wet processing or thermal evaporation. Device configurations are single layer, bilayer heterojunction, and bulk heterojunction, and those type of devices are fabricated with the inter-diffused bi-layer heterojunction as intermediate between the bilayer and the bulk

heterojunction, so the single layer consists of only one active material, the other superstrate configuration based on two different types of materials: electron donors (D) and electron acceptors (A) respectively. In the organic DA solar devices, the photoinduced electron transfer occurs from the excited state of the donor to the LUMO of the acceptor, which has to be an excellent electron acceptor with a stronger electron affinity [25]. After separating the charge, both the electron and hole have to transport out to the opposite electrodes, the cathode, and the anode, respectively. Hence, direct current can be generated to an external circuit.

1.1.3.3 Perovskite Solar Cells

Perovskite solar cell (PSC), which is one of the organic solar cells are the perovskite-structured material as an absorber layer depended on a solution-processed tin or halide. It is a desirable choice for commercial applications because this type of PV technologies are very cheap and can be easily scaled-up to large area manufacturing [26]. Perovskite solar cells have emerged and developed as one of the most favorable future solar cell devices due to the rapid advancements in efficiency. Therefore many research groups have revealed considerable interest in developing Perovskite solar cell. The advantages like flexibility, lightweight, and semitransparency, which are shown some of the valuable properties of perovskites [27].

1.1.3.4 Quantum Dot Solar Cells

For the physics design of quantum dot solar cell, this PV technology utilizes quantum dots within the absorber material. Thus, the materials include typical silicon, CdTe, and CIS which can be switched by a quantum dot material itself, and it has a high optical energy bandgap which is utilized to tune various range of energy levels [28]. Although the efficiency of the quantum dot devices was still as low as 10%, it has brought up intriguing attention to the researchers because of its versatile properties, lightweight, and potential for high efficiencies.

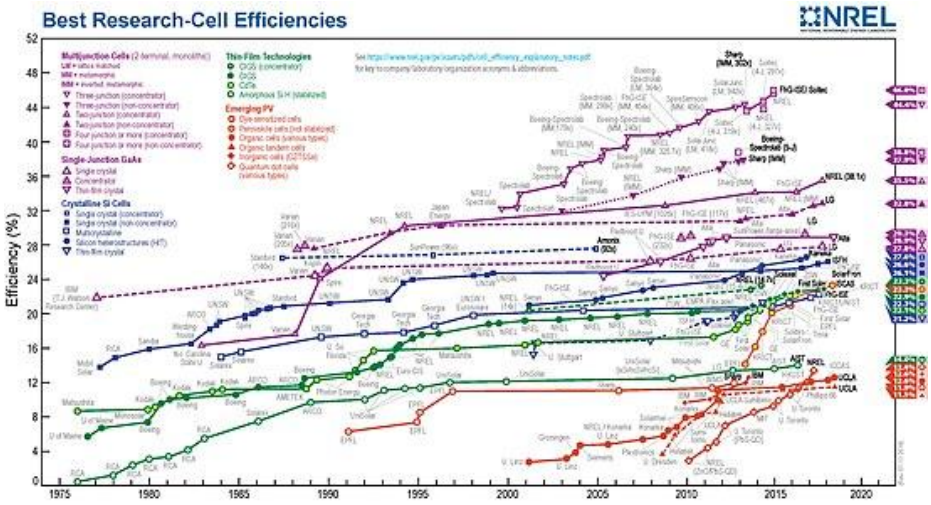


Figure 5 The devices efficiencies table of solar cells in recent research [29].

1.2 The Reason for CdTe

The three main reasons for the utilization of CdTe thin film solar cells are described below:

- Direct bandgap materials in the range of 1.1-1.45 eV for larger photo-electronic conversion.
- A high optical absorption coefficient ($10^4 – 10^5$ cm^{-1}) in the sunlight spectrum (400-1000 nm).
- The ability to provide both n and p-type material with the use of suitable dopants.

Cadmium telluride (CdTe) solar cells have become considerably high demanding as a massive PV technology market among the solar cells. Regardless of the PV market has been still dominated by silicon solar cells, CdTe now rises around a 10% market share [30], and it is believed to call the first of the second generation thin film technologies to jump to massive deployment effectively. Due to a direct 1.5 eV bandgap, decent optical absorption around $1 \times 10^{4-5}$ cm^{-1} [31], and pure binary phase chemistry, which results in eminently scalable technology for CdTe devices. Cell efficiencies for lab-scale devices have now exceeded 22.1% [32], and large scale modules have approached 18.6%, competitive with multi-crystalline silicon modules (Figure 5). It is also now purported to be relatively lower cost per watt technology, and be the less carbon-intensive in the manufacturing processes. CdTe solar cells have still considerably researched in recent years, but there have several critical technical challenges during the development if the issue can be

overcome. It is assumed that the cell performance could improve the conversion efficiencies approaching the theoretical maximum of 32%. This dissertation will discuss the current state of the CdTe PV technology and reviewing each of the critical challenges in turn before looking at research that is a focus on further development.

CHAPTER 2

SEMICONDUCTORS AND SOLAR CELLS

2.1 Semiconductors

Semiconductors are substances which have the conductivity between that of insulators and metals. Silicon (Si) material is the most popular and abundant elemental semiconductor and has been extensively developed and advanced by the microelectronics industry. In general, the combination of group II and VI elements, and group III and V elements are among the most common compound semiconductors, respectively. For example, gallium arsenide (GaAs) and gallium nitride (GaN) are typically Group III-V semiconductors, and cadmium telluride (CdTe) and cadmium selenium (CdSe) is defined as group II-VI. Semiconductors are the foundation of modern application on electronic devices due to the variation of conductivity by employing different impurities in the crystal lattice of semiconductor materials. The controllable atomic level of impurities incorporated in a semiconductor material and which leads to change in its electrical characteristics is the so-called doping process. Based on the type of majority charge carrier – electrons or holes - the semiconductor can be n or p-type. For example, adding phosphorus, a group V element, into Si produces a free electron, increasing the concentration of free electrons, as shown in Figure 6 (a). Due to the phosphorus as a donor element, this incorporation procedure is called n-type doping. In addition, p-type doping Si is achieved if a group III element, such as boron, is incorporated into Si (see in Figure 6 (b)). In order to increase in the hole density concentration, doping boron atoms, or in general p-type dopant elements are called acceptors.

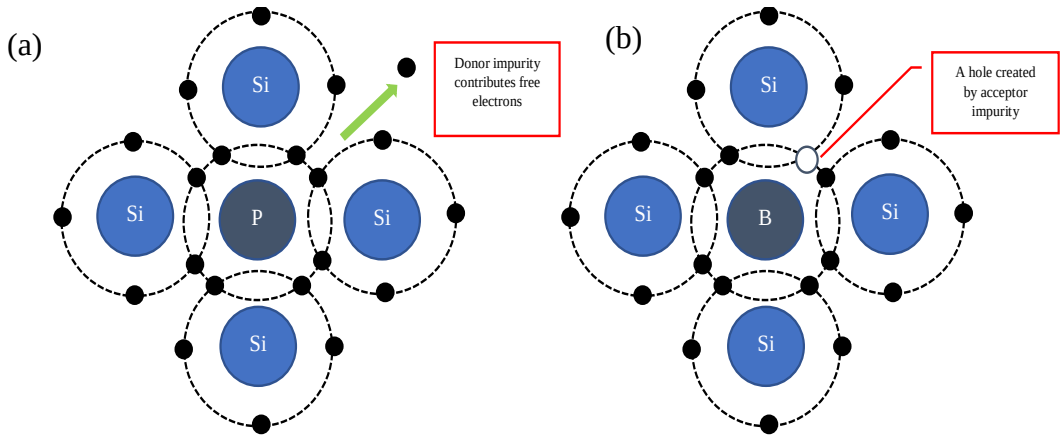


Figure 6 The (a) n-type and (b) p-type impurity doping Si semiconductor materials.

2.2 P-N Junctions

The most common semiconductor devices consist of as a minimum of one p-n junction as part of the device. The p-n junction is the basic building block of devices like diodes and transistors. When p-type material (majority carriers are holes) directly contacts with n-type material (majority carriers are electrons), the devices are determined as a p-n junction which is shown in Figure 7. The n and p- regions are separated by an interface which is named the metallurgical interface. Initially, at this interface, the area contains a higher concentration of electron and hole. Majority carrier holes from the p-region will begin diffusing into n-region, and majority carrier electrons from the n-region will begin diffusing into the p-region. This transportation of charge carriers establishes the diffusion current in the p-n junction. Electrons are transported out from the n-region and holes transporting out from the p-region with the uncompensated charge of donor and acceptor ions respectively. This uncompensated charge produces an electric field named the built-in field for the operation of the p-n junction. The built-in field happens in a region at the junction which is defined as the depletion region, due to the fact that it is now depleted of free electrons and holes, and a drift component of current is formed in the opposite direction to the diffusion current. The electric field continues to build up as equilibrium is reached, and the intrinsic current is zero. The Fermi energy level remains constant

throughout the system under the thermal equilibrium state. In the temperature at 0K, the maximum energy occupied by an electron is associated with the Fermi energy level. In Figure 8, the basic energy band diagram is shown for the p-n junction under equilibrium. The depletion region by an energy qV_{bi} is revealed the bands bend, and this energy is defined as the built-in-potential. The following equation can express the built-in-voltage under thermal equilibrium:

$$V_{bi} = \frac{kT}{q} \times ln\left(\frac{N_A N_D}{{n_i}^2}\right) \qquad (1)$$

where N_A and N_D are the doping concentrations for acceptor (hole) and donor (electron), n_i is the intrinsic carrier concentration, k is Boltzmann's constant, and T is the absolute temperature. Applied voltage (V_A) appears across the depletion region, forcing the separation of Fermi levels in the opposite direction, while the potential barrier decreases from V_{bi} to (V_{bi}-V_A). If the diffusion and recombination process occurs the movements are shown that the majority of holes from the p-region is drifted to the n-region and majority carrier for electrons from n-region is drifted to the p-region. The potential offset is increased as the function of the V_A when the reversed bias is applied on the p-n junction. In the semiconductor behavior, the potential offset is increased by reducing the number of majority carriers. It is believed to create a difficulty to the flow of charge carriers so that causing the minimal electric current to cross through the p-n junction. Figure 9 shows the p-n junction under reverse bias. The following relationship gives the current diffusing through a p-n junction under forward or reverses bias:

$$I = Is \times \left(e^{\frac{qV}{AkT}} - 1\right) \qquad (2)$$

where I_S is the "reverse saturation current" and A is the "diode quality factor." The values for A are generally between the range of 1 to 2. For A=1, the transportation of the current is dominated by diffusion while, as A=2 is dominated by recombination [33].

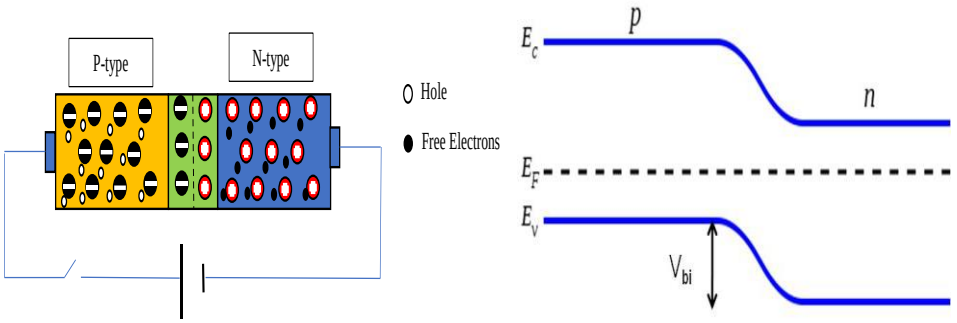


Figure 7 A p-n junction devices consist of p-type material (hole) and n-type material (free electron).

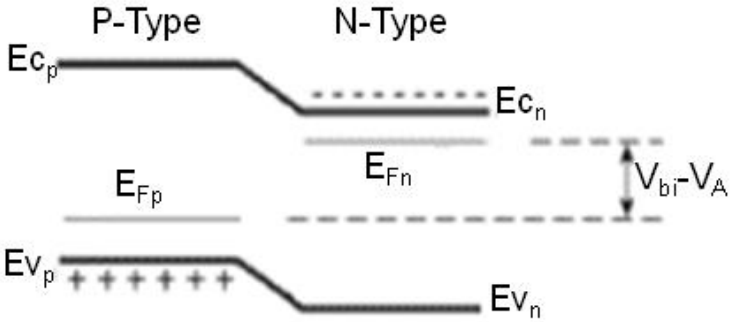


Figure 8 The basic energy band diagram of the p-n junction under equilibrium state.

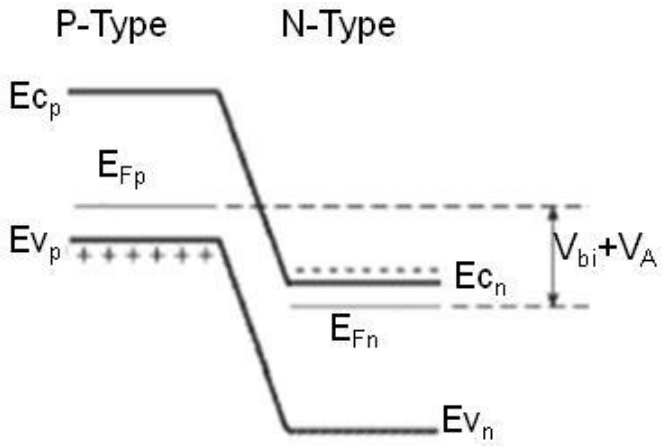


Figure 9 The energy band diagram of the p-n junction under reverse bias.

2.3 Metal-Semiconductor Contacts

The metal-semiconductor (MS) contact is an essential element for the performance of common semiconductor devices. An MS junction is formed when a metal is brought in contact with a semiconductor. MS contacts are categorized into two different types that are widely used in semiconductor devices:

- Rectifying Schottky barriers.
- Ohmic contacts.

2.3.1 Schottky Barriers

Before contacting metal and n-type semiconductor materials are defined for the basic energy band diagrams which are revealed in Figure 10. The vacuum energy level is called E_0 and determines as the energy of a completely free electron. The work function Φ_M is for metal material, and the Φ_S is known as n or p-type semiconductor material. The band energy can change the location from the vacuum level to the Fermi energy level (E_F) is defined for the work function of semiconductor material. When it comes to the given semiconductor materials, depending on different doping impurity level causes the various value of the work function. However, the location of the bands does not affect by the doping impurity, especially in the vacuum level. Another important value in the Schottky barrier is the parameter χ, which is called the electron affinity energy, and this value defines the location of the bottom of the conduction band to the vacuum energy. From Figure 10, the Fermi level of n-type material show a higher location than the metal materials, and it generally means the energy of electrons has more than the energy of electrons in the metal. Electrons will begin to diffuse from the semiconductor to the metal material until the Fermi energy levels of the two materials align with the same location, and the device becomes equilibrium after the metal directly contact with a semiconductor. The energy band

diagram of the device under an equilibrium state is shown in Figure 11. Electron is diffused from the semiconductor to the metal and establishes a depletion region at the semiconductor junction. The doping concentration can affect the various extent of band bending in the depletion region between the Fermi levels of the metal and semiconductor materials. The energy barrier is created by electrons moving from the semiconductor to the metal. In between the metal and the semiconductor is shown the transportation of electron that is defined as a different level of the barrier, Φ_B is given by the variation between the metal Fermi level and the semiconductor electron affinity:

$$\Phi_B = \Phi_M - \chi \qquad (3)$$

where metal-semiconductor Schottky barrier band diagram under equilibrium is shown in Figure 11. The number of electrons diffused from the metal to semiconductor so that the current in the metal-semiconductor junction can be anticipated. The Applied Voltage (V_A) is given from the metal to the n-type materials, similar to the p-n junction. The metal-semiconductor is applied for forward and reverse bias, which is shown in Figure 12 (a) and (b). When the contact is applied for the forward bias ($V_A > 0$), the energy barrier in the depletion layer is equal to $q(V_{bi}-V_A)$. Thus, due to the low of the barrier, the electrons can be able to transport from the semiconductor to the metal material. It results in the more current diffuse from metal to semiconductor under the forward bias voltage. However, the electron in the metal has the same exactly barrier (Φ_B) as under the equilibrium state. In comparison, the height of the energy barrier intends to increase to $q(V_{bi}+V_A)$ when the V_A is applied for reverse bias ($V_A < 0$). Due to the height of the barrier, the amount of electrons is more difficult to transport into the metal. Due to the unchanged of Φ_B barrier, the same amount of electrons diffuse from the metal to semiconductor under the forward bias case. The reverse current transfer from semiconductor to metal.

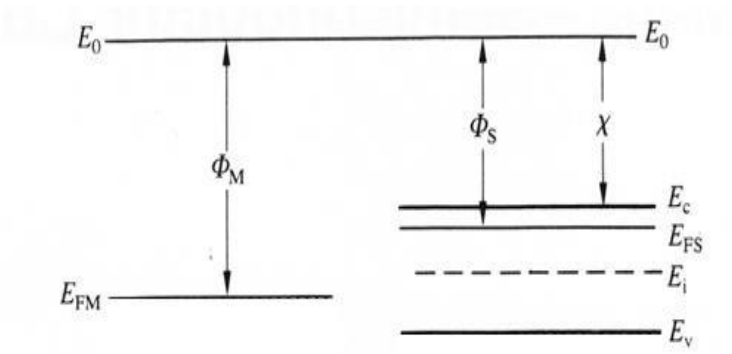


Figure 10 The energy band diagrams of a metal and an n-type semiconductor before both come into contact.

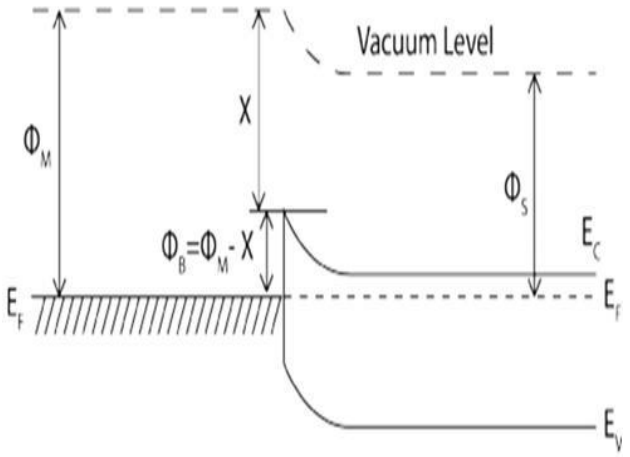


Figure 11 The energy band diagrams of a metal and an n-type semiconductor after contact.

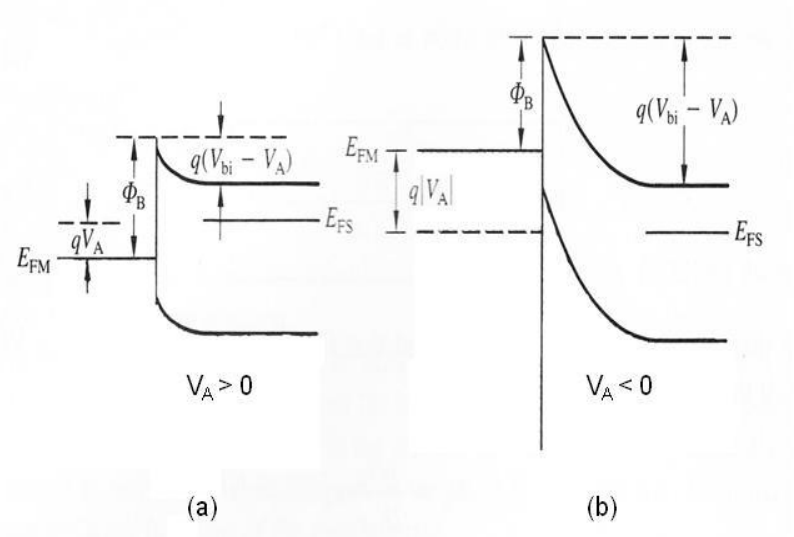


Figure 12 The metal-semiconductor contact (a) under forward and (b) reverse bias.

2.3.2 Ohmic Metal-Semiconductor Contacts

As the work function of semiconductor is larger than that of the metal ($\Phi_S > \Phi_M$), the band diagram of metal and an n-type semiconductor is shown in Figure 13. If two materials contact together and form an ohmic metal-semiconductor, the electron will easily transfer from the metal to the n-type semiconductor. In the ohmic contact, the semiconductor interface shows more occupied electrons so that an electron concentration is typically higher than in the bulk region. The surface charge generates free electrons in the semiconductor. This behavior is different from the Schottky contact, where positive donor ions occupy the surface as a barrier and form the depletion region in the interface. Because of the ohmic contact, the depletion region has not appeared so the reduction of voltage across the metal-semiconductor junction can be ignored under any voltage bias. The transportation of electrons is shown in Figure 13, and the conduction band of the semiconductor gives the idea for no a barrier along with the metal. On the other hand, as the work function value of the metal is larger than the p-type semiconductor material ($\Phi_M > \Phi_S$), an ohmic contact can also be established between both materials. If metal materials with the desired work function to achieve ohmic contact are not available, different approaches have been utilized to achieve "pseudo-ohmic" contacts. For example, The width of the depletion region can be reduced by heavily p-type doping for the material which creates a p+ region. It is a result that shows in Figure 14(a), due to the semiconductor under a negative voltage, the electrons can tunnel through the barrier from the metal. In comparison, Figure 14(b) shows the same behavior as the semiconductor is applied for the positive voltage. Electron in the semiconductor can be diffused as similar as ohmic contact devices. Therefore electrons can overcome the decreased barrier and proceed the tunneling effect through the barrier.

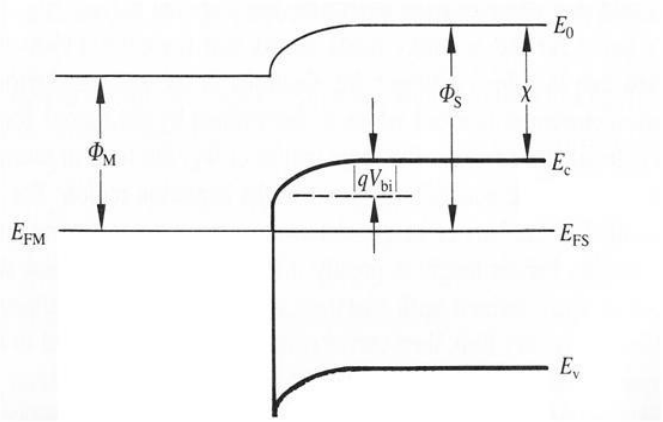


Figure 13 Band–diagram of an ohmic metal-semiconductor contact.

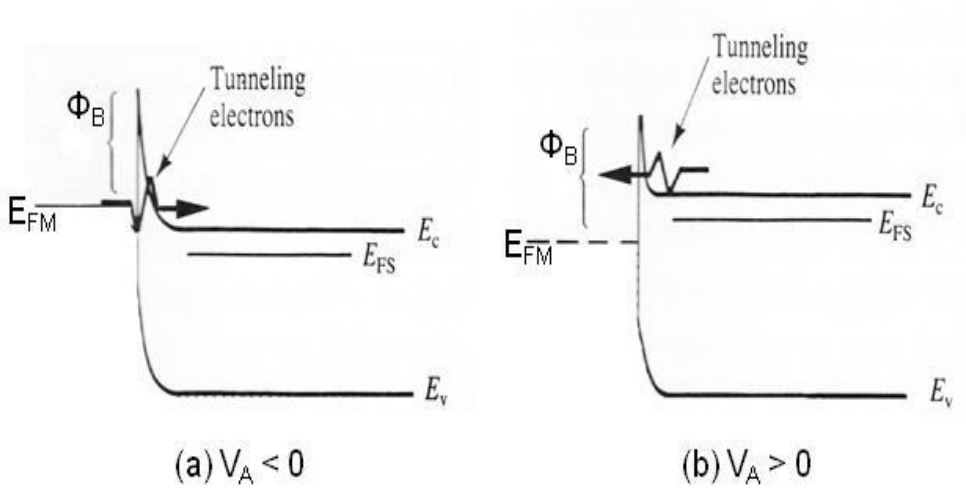


Figure 14 The case where (a) negative and (b) positive voltage is applied to the semiconductor.

2.4 Heterojunctions Semiconductor

If the semiconductor material that forms the p-n junction is the same, this type of junction is determined as a homojunction. However, if two different semiconductor materials are used to form a junction, the junction is named as a heterojunction device. Figure 15 shows the energy band diagrams of an n and p-type semiconductors before contact. E_{gp} and E_{gn} are the bandgaps of n or p-type materials, Φ_n and Φ_p are the work function for each, and χ_n and χ_p are the electron affinities of n and p-type semiconductors respectively. ΔE_v gives the variation of value between the two valence band energies, which is called valence band offset, and ΔE_c gives the difference between

the two conduction bands is defined as conduction band offset. The energy-band diagrams of an n and p-type heterojunction before contact is shown in Figure 15. When the Femi levels in both materials are aligned together, holes from the p-region and electrons from n-region have to diffuse across the junction in order to form a depletion area. The depletion region in each n and p semiconductors reveal different potential which is related to the value of built-in potential barriers on each side of the junction. The total built-in potential barrier is given by

$$V_{bi} = V_{bin} + V_{biP} \qquad (4)$$

where the conduction (ΔE_c) and valence (ΔE_v) band offset value, in Figure 16 given by equations, 5 and 6 respectively are relied on an ideal abrupt heterojunction.

$$\Delta E_c = \chi_P - \chi_n \qquad (5)$$

and

$$\Delta E_g = E_{gp} - E_{gn} = \Delta E_c + \Delta E_v \qquad (6)$$

where the ΔE_g is equivalent to the difference of energy bandgap of p and n-type materials as similar as the values of the combination of ΔE_c and ΔE_v ideally, but for experimental process shows the different case due to the presence of interface states at the junction.

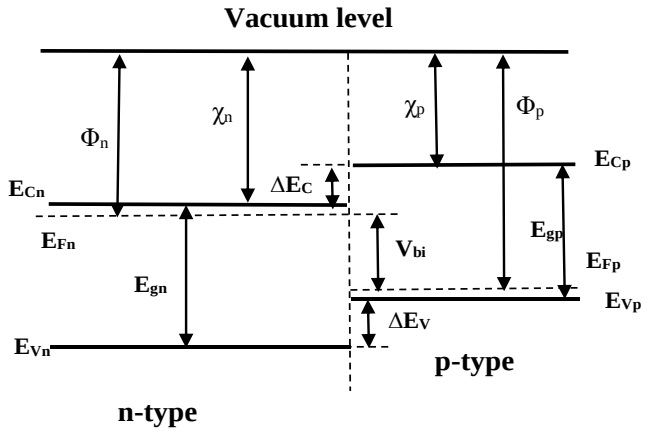


Figure 15 The energy-band diagrams of an n and p-type heterojunction before contact.

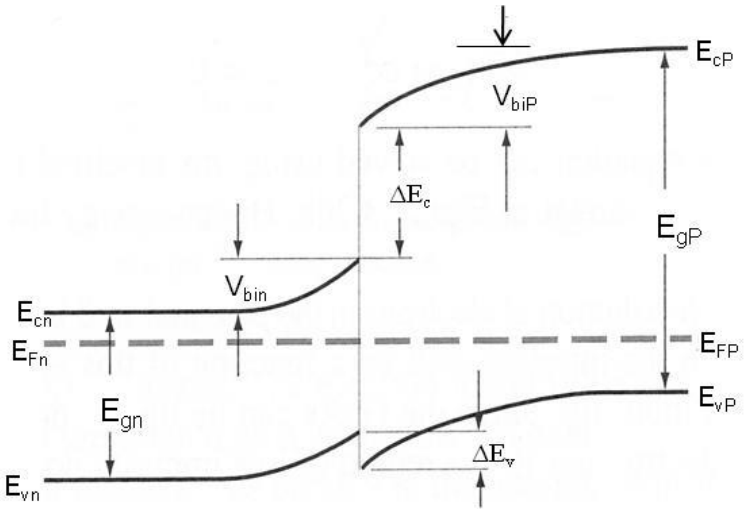


Figure 16 The energy-band diagrams of an n and p-type heterojunction after contact.

2.5 Solar Cells

A solar cell is one of crucial electronic device which can directly convert from sunlight into electricity power by the effect of photovoltaic based on the conversion efficiency. Solar cells are designed by using different device configurations and employing single-crystalline, polycrystalline, or amorphous structures as the different forms of semiconductor materials. Chapin, Fuller, and Pearson, who developed the first p-n junction silicon solar cell in 1954 was an incredible finding in modern technology [34].

2.5.1 Solar Spectrum

From Table 2.1, the different intensity of solar radiation is shown the values which are defined as the solar constant at the average and given angles of the earth from the sun in the free space. For air mass zero (AM0), the solar constant is associated with the solar radiation outside the earth's atmosphere; thus the value is utilized as a standard for satellite and space applications. As measuring data is taken from outside of earth which have generated the given accepted average value of 135.3 mW/cm^2. On earth, at sea level with the sun at zenith, the intensity level is reduced to 100 mW/cm^2 as the AM1 sun radiation from the energy of sunlight. AM1.5 is the adopted terrestrial standard used for comparison between different solar cells for terrestrial applications.

The given vertical angle (zenith) between the sun and atmosphere with the ratio of path length for the sunlight is calculated as Air Mass (AM) coefficient. The AM equation shows the relationship

$$AM = (\cos\theta)^{-1} \qquad (7)$$

where θ is the zenith angle, AM1.5 refers to a zenith angle of 48.2° which results in the value of 83.2 mW/cm^2. As the value is close to the maximum received at the earth's surface with approx. 100 mW/cm^2 was defined as a standard AM1.5G. The energy of absorption edge on a semiconductor in terms of wavelength can be attained from the relationship:

$$\lambda = \frac{c}{\nu} = \frac{h\,c}{Eg} = \frac{1.24}{h\,\nu} \quad \mu m \qquad (8)$$

where ν is the frequency in Hertz, c is the velocity of light in m/s, and hν is the photon energy in electron voltage (eV). Figure 17 shows a typical spectral response under illumination in ideal and practical Si solar cells.

The energy-band diagram of a p-n heterojunction device is shown in Figure 18. After illumination for the device, light can penetrate through the wide-bandgap material (known as window layer) as photons have lower energy (hν) than $E_{gn,}$ in addition, the light will be absorbed in the narrow-bandgap material (known as absorber layer) due to photons with energies higher than E_{gp} respectively, and generating the free electron and hole pairs at the junction. Carriers created in the depletion region are readily collected due to the electric field, while those generated outside the depletion region must first diffuse to the depletion region before they collected and contributed to a photocurrent. In heterojunction solar cells of this type, it is desirable that the window layer has significantly larger E_g than the absorber in order to allow photons of all wavelengths to reach the absorber.

Table 2.1 The intensity of solar radiation in free space.

Air Mass #	Input power (mW/cm^2)
AM0	135
AM1	100
AM1.5	83.2
AM1.5G	100
AM2	69.1

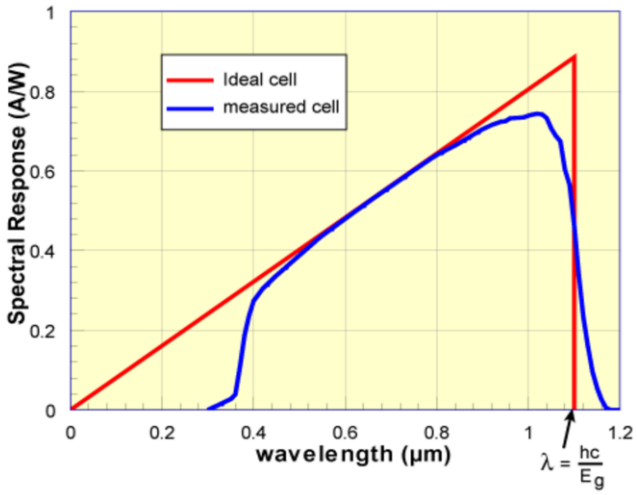


Figure 17 A typical spectral response under illumination by the sun in ideal and practical Si solar cells [35].

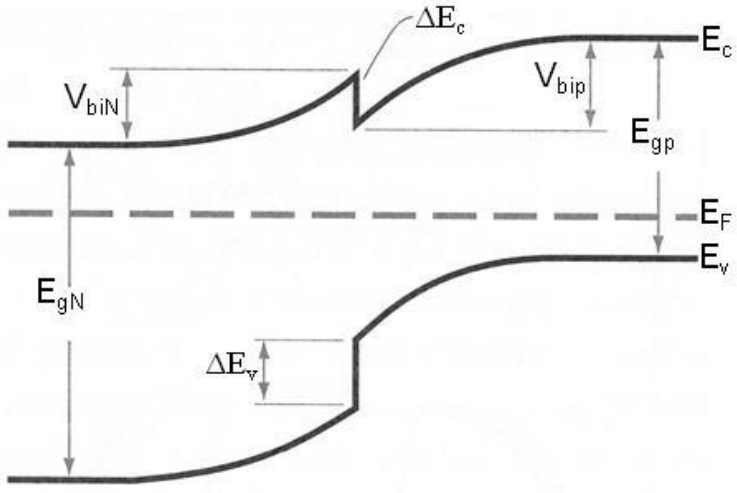


Figure 18 The energy-band diagram of a p-n heterojunction solar cells.

2.5.2 Solar Cell Parameters

The most significant parameters of solar cells include the values of the short circuit current (I_{SC}), open circuit voltage (V_{OC}), fill factor (FF), and the energy conversion efficiency (η) which are utilized for evaluating performance. Figure 19 shows the I-V characteristics of a solar cell in the dark and after illumination for I-V curves. The total current is given by

$$I = I_s \times \left(e^{\frac{qV}{AkT}} - 1\right) - I_L \qquad (9)$$

where I_s, is the reverse saturation current, and I_L is the light generated current. In the light I-V, the value is generated for the negative current, which points out that the solar cell can deliver electricity to a load. Thus, I_{SC} is associated with the amount of current through the circuit when the open circuit voltage is equal to zero (V=0). In equation 9, result in $Isc=I_L$. On the other hand, as short circuit current is equal to zero (I=0), from equation 10 is defined as the load is infinite and is given with relationship:

$$V_{oc} = \frac{AkT}{q} \times \ln\left(\frac{I_L}{I_s} + 1\right) \qquad (10)$$

From Figure 19, Imax and Vmax are the current and voltage are associated with the maximum power which can be generated by the solar cell. The maximum possible area of Pmax= Imax * Vmax for a given current-voltage curve determines the FF, which is given by the following relationship:

$$FF = \frac{Vmax\ Imax}{Voc\ Isc} \qquad (11)$$

The three parameters V_{OC}, I_{SC}, and FF are used for evaluating the conversion efficiency η for solar cells performance which is provided by the following expression

$$\eta = \frac{Pmax}{Pin} = \frac{Voc\ FF\ Isc}{Pin} \qquad (12)$$

where Pin, is the incident light power. The efficiency of a solar cell is influenced by series (R_s), and shunt (R_{sh}) resistance, as demonstrated in Figure 20 for the equivalent circuit of the solar cell. The series resistance is shown zero in the ideal solar cell, and the shunt resistance is defined as infinite. A finite shunt and series resistance characterizes all real solar cells. By using the series and shunt resistance as a calculation for equation 13 shows the relationship

$$I = I_L - I_0 \exp\left[\frac{qV}{nkT}\right] - \frac{V}{R_{SH}} \qquad (13)$$

The value of series resistance is affected by the quality of contact and bulk of the device material. In addition, the decreased shunt resistance is attributed to the defect issue, including pinholes, grain boundaries, and other dislocations in the solar cell. A low shunt resistance leads to high leakage currents, which reduce the values of Voc and FF. Moreover, non-ohmic effects (such as non-ohmic contacts) can also reduce the FF due to roll-over in the I-V characteristics of solar cells. Hence, in order to improve the overall efficiency of solar cells, then the shunt resistance must be maximized, and the series resistance must be minimized.

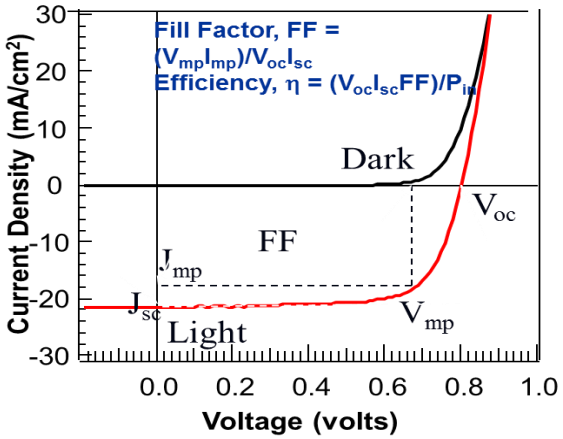


Figure 19 The I-V characteristics of a solar cell in the dark and under illumination.

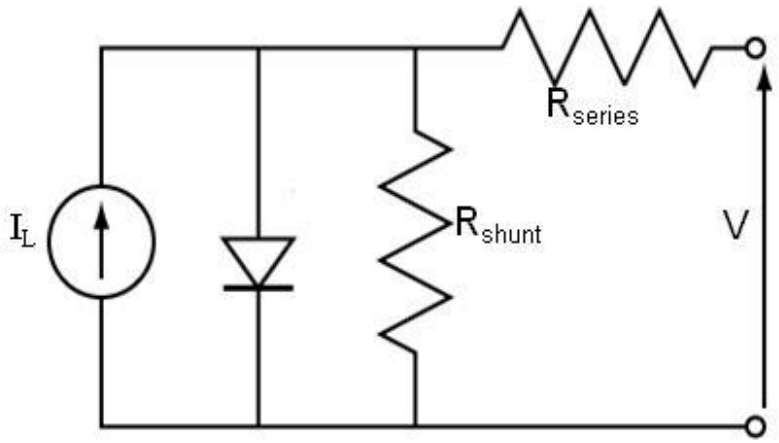


Figure 20 The equivalent external circuit for a solar cell.

CHAPTER 3

THE CDTE BASED THIN FILM SOLAR CELL

3.1 Traditional Architecture – CdTe/CdS

The conventional device architecture is shown in Figure 21 for CdS/CdTe thin film solar cells. After a glass substrate deposits a transparent contact (TC) on the top of it, the deposition of window layer, absorber (CdTe), and the back contact are fabricated by different deposition techniques.

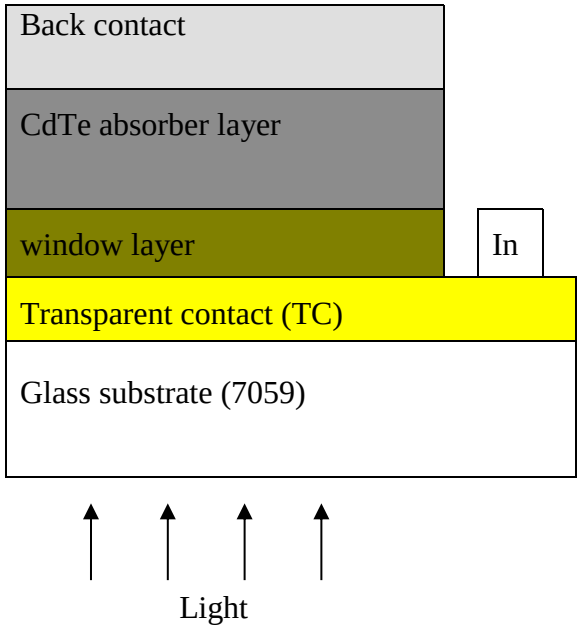


Figure 21 CdTe/CdS traditional architecture solar cell.

3.2 Transparent Glass Substrate

According to the literature survey, CdTe solar cells have been developed and fabricated in the high substrate temperatures (~580 °C) by Close Spaced Sublimation (CSS) for the highest efficiencies [36]. Alkali-free glass (Corning Eagle X2000) is often used in research as it can be tolerant for these high temperatures fabrication processes, and remain high optical transparency.

Nevertheless, in manufacturing fab, soda lime glass (TEC 10, etc) is preferred due to the material's low price.

3.3 Transparent Contacting Oxides (TCOs)

Thin film solar cells are required to have transparent semiconductor materials as front contact. Since most of these are oxides, they are referred to as transparent conducting oxides. In order to form an ohmic contact with the CdS layer at the junction, the transparent oxide contact needs to remain the electron affinity around 4.5eV. However, as the electron affinity of the TCO is higher than the CdS (4.5eV), a Schottky contact can form. TCO's are heavily doped (degenerate), and their Fermi energy is near their conduction band.

TCO is deposited as a front contact have to follow several vital characteristics below:

- Resistivity is lower than 10^{-4} Ω cm.
- Higher transmission in the wavelength between 300-900 nm.
- During high-temperature fabrication need to remain chemical stability.

TCO materials typically act like insulators due to the wide optical bandgaps property as the materials are intrinsic, stoichiometric, and undoped TCO. By harnessing the extrinsic doping, the higher conductivity of the TCO can be anticipated. Due to the donor impurities in the oxide, the substitution of valence cations for the materials can increase the n-type TCO conductivity by improving the electron concentration. Fluorine doped tin-oxide SnO_2: F (FTO), tin-doped indium oxide In_2O_3:Sn (ITO) and cadmium stannate Cd_2SnO_4 (CTO) are frequently used as TCO's for CdTe solar cells. As the formation of oxygen vacancies act as native defects, the most common TCO materials have a tendency to be an n-type semiconductor. The transmission and resistivity are shown in Table 3.1 for the most favorable TCO materials. The decent optical transparency approx. 85% and excellent n-type conductivity are revealed as metallic oxides. In the recent

research, utilization of bi-layer TCO/buffer layer can improve the efficiency of the solar cell that the TCO has to comprise of a higher conductivity following by a higher resistivity transparent oxide (HRT) as a buffer layer [37]. As the possible solar cells devices have the window layer as CdS layers, the use of HRT as a buffer layer leads to enhance considerably for maintaining decent FF and Voc. The intention of utilizing the HRT as a buffer is suggested to act as a high bandgap extension of the thinner CdS and alleviating the crystal mismatch between TCO and CdS layer [38]. The HRT also can prevent shunting effect and current leakage between TCO/CdS due to high- ρ layer as an insulator.

Table 3.1 The characteristics of transparent conducting oxides and buffer layers.

Material	Resistivity (Ω-cm)	Transparency (%)
SnO_2	8×10^{-4}	80
SnO_2:F	$3x\ 10^{-4}$	84
In_2O_3:Sn	2×10^{-4}	85
Cd_2SnO_4	1×10^{-4}	92

3.3.1 Fluorine Doped Tin Oxide (SnO_2:F)

SnO_2 (TO) is a promising material used as common transparent oxides. TO films are typically deposited by Chemical Vapor Deposition and R.F sputtering [39, 40]. The gas or liquid precursors are used as reactants supply in the deposition chamber, and a film is deposited on the substrates during CVD fabrication process. The common use of inorganic and metal-organic as precursors materials include tin tetrachloride ($SnCl_4$), dimethyl tin dichloride ($(CH_3)_2SnCl_2$), tetramethylene ($Sn(CH_3)_4$), and oxygen (O_2) [41]. As well known, the substitution of Oxygen-vacancies can primarily define the values of n-type conductivity; however, the TO films is not

suitable for use as front TCO's on thin film solar cells due to its high resistivity in the electronic property. When the TO films use the precursors containing HF (hydrogen-fluoride) acid, the conductivity can be significantly improved. In order to obtain higher conductivity, TO film can be extrinsically doped with fluorine in the CVD fabrication process.

FTO films can also be formed by R.F sputtering technique, which has the process of CHF_3 in the range 1-10% concerning the total Ar + CHF_3 pressure during the deposition. The excellent resistivity can approach approximately 4 x 10^{-4} Ω-cm by using R.F sputtering.

3.3.2 Tin Doped Indium Oxide (ITO)

One of the accessible materials is Indium tin oxide (ITO), which can be deposited by numerous techniques such as D.C and R.F sputtering, chemical vapor deposition, and vacuum evaporation. ITO act as front contact oxide for CdTe thin film solar cell. The substitution of the indium ion tends to provide an additional electron to form n-type doping in the conduction band by using Tin as a cationic dopant in the In_2O_3 lattice. The highest resistivities are reported by R.B.H. Tahr et al. as lower as 2x 10^{-4} Ω-cm, which are deposited by utilizing R.F sputtering process [42].

The R.F sputtering process is reported by N. Romeo et al. that the different stoichiometries are depended on different preparing targets [43]. In_2O_3 containing 1, 2, 4, and 10% weight of SnO_2 was utilized. Depositions proceeded by using various ambient environments. By incorporation of mixing gas Ar + O_2 ambient during the process, the ITO films were deposited with the two different Oxygen and hydrogen each partial pressures under 3-30% and 1.5-15%, respectively. The most ITO films remain extremely low resistivity approx. < 2 x 10-4 Ω-cm. Due to the low activation energy of tin for n-type doping, it is suggested that ambient gas and the different stoichiometry of

targets did not affect the conductivity of the films overall, and the doping level does not define by oxygen vacancies as well.

3.4 The Cadmium Sulfide (CdS) Layer

The conventional CdS/CdTe thin film solar cell commonly use the CdS material as a window layer. Thus, CdS acts as n-type materials in order to form a p-n junction following by p-type CdTe. The light allows penetrating to CdS layer between the visible solar spectrum (> 500nm), due to an energy bandgap of CdS (2.42eV).

The short circuit current (Jsc) shows the maximum theoretical data up to 26 mA/cm^2 in the best traditional CdS/CdTe solar cells. In the downside, the CdS layer cause absorption in the short wavelength, which is equivalent of approx. 8 mA/cm^2 under AM1.5 illumination [44]. Thus, the significant reduction of the solar spectrum appears below the 510nm, this wavelength that is corresponded to the actual energy bandgap for CdS material. The most of photo-generated carriers in this layer are not effectively formed the photocurrent, due to low hole lifetime, and high recombination center. Thus, the window loss is expected to find in the wavelength range from 300 to 510 nm. The promising approach is to reduce the thickness of the CdS layer as lower as possible for alleviating the window losses. The quality performance of fabrication process maintain the uniform and non-particle film to prevent the formation of pinholes at the junction of the device, so it is believed in eliminating the shunting effect by establishing the parallel junction between TCO and CdTe. Chemical bath deposition (CBD) and Close Spaced Sublimation (CSS) [45], are the most promising deposition techniques for thinner (<100nm) uniform CdS layers to reduce the window lost in the solar spectrum.

The lattice mismatch between CdS and CdTe is ~9%, which can lead to the formation if the high concentration of interface states at the interface. The formation of an interfacial layer

$CdTe_{1-x}S_x$ layer (Te-rich alloy) is contributed to creating high quality and efficient CdS/CdTe junctions. The effect of $CdS_{1-x}Te_x$ alloy (S-rich) has been discussed in the following session of post-annealing $CdCl_2$ treatment [46]. The main reason for having high efficiency devices can reduce the interfacial defect density between CdS/CdTe [47]. There are numerous deposition techniques for the deposition of CdS layer such as Chemical Bath Deposition (CBD) [48], Close Spaced Sublimation (CSS) [49], and R.F sputtering [50].

3.4.1 CdS via Chemical Bath Deposition (CBD)

The most common reason is suggested to use the CBD process, due to low manufacturing price for depositing CdS which is fabricated to achieve a decent quality of CdS layer in higher conversion efficiency CdS/CdTe solar cells. The CBD process includes cadmium acetate is used as cadmium source. Thiourea is utilized as a sulfur source, ammonium acetate (NH_4AC) and ammonium hydroxide (NH_4OH) are used as buffers to maintain the PH value. The SnO_2: F or ITO coated glass substrates are immersed in DI water, and it is important to remove bubbles on the surface during the deposition process, which should completely maintain the substrate face up. The temperature needs to be controlled between 75-95 °C during the CBD process. The thickness of CdS can be tuned by various deposition time. J. Herrero et al. [51] proposed the possible reactions as follows:

$$Cd(CH_3COO)_2 \leftrightarrow Cd^{2+} + 2CH_3COO^-$$

$$NH_3 + HOH \leftrightarrow NH_4^+ + OH^-$$

$$Cd(NH_3)_4^{2+} + 2OH^- \leftrightarrow [Cd(OH)_2(NH_3)_2] + 2NH_3$$

$$[Cd(OH)_2(NH_3)_2] + SC(NH_2)_2 \rightarrow [Cd(OH)_2(NH_3)_2SC(NH_2)_2$$

$$[Cd(OH)_2(NH_3)_2SC(NH_2)_2] \rightarrow CdS_{(S)} + CN_3H_5 + NH_3 + 2HOH$$

It is known that the as-deposited CdS layer is expected to consist of two different types of crystalline structures, which are the cubic and the hexagonal, respectively. The post-annealing or following fabrication annealing process at the temperatures around 500°C allows the CdS film which is deposited by CBD to increase the preferential percentage of hexagonal crystal orientation. It is believed to give higher stability than the cubic structure.

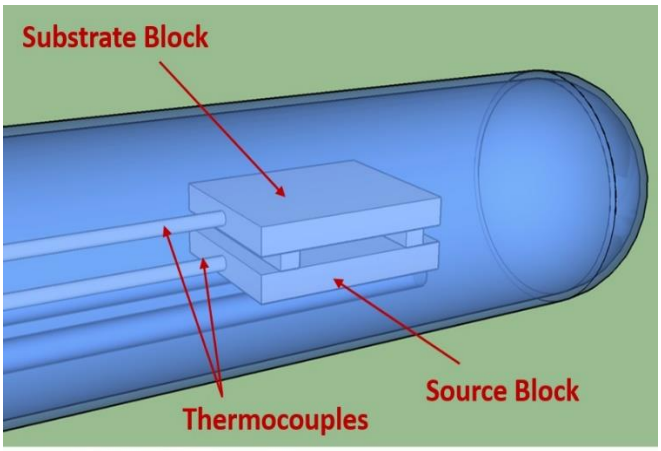


Figure 22 The diagram of Close Spaced Sublimation (CSS) system.

3.4.2 CdS via Close-Spaced Sublimation (CSS)

From Figure 22**,** Close Spaced Sublimation (CSS) is utilized for depositing the CdS film to maintain precise thicknesses, and the process is based on the reversible dissociation of CdS under higher thermal temperatures. The CSS for the methodology of the process is reported by D. Marinskiy et al. [52], and the CdS powder can be dissociated and recombined on the substrate to generate the CdS film, thus understanding the effect of the CSS CdS can provide the better performance on the CdS/CdTe solar cells. The CdS layer, which is fabricated by the CSS method, were reported the highest conversion efficiency of samples up to 15%. CdS layer was deposited in the ambient environment of He and partial pressures of He and O_2 during the fabrication process on the samples. Increased the partial pressure in the oxygen ambient was reported a lacking of sulfur vacancies, and it is believed to be the result of incorporating O_2 in the CdS film. In order to

improve the performance of solar devices, the CdS film should proceed under post-annealing treatment.

3.5 The Cadmium Telluride (CdTe) layer

Cadmium telluride is one of the essential II-IV semiconductors which contain excellent electronic and optical properties for acting as an ideal active or absorber layer in the thin film solar cells. To understand the effect of the bandgap of materials, the theoretical efficiency-bandgap relationship shows in Figure 23. The maximum efficiency corresponds to the bandgap of 1.45 to 1.5 eV. When the CdTe act as absorber layer due to the ideal bandgap of 1.45ev, the solar cell conversion efficiency can be effectively maximized. CdTe is a direct bandgap material with a high absorption coefficient > 5×10^4 cm^{-1}. Due to this high absorption coefficient, the CdTe only need a few micrometers (approx. 2μm) of material is sufficient to absorb the entire incident light.

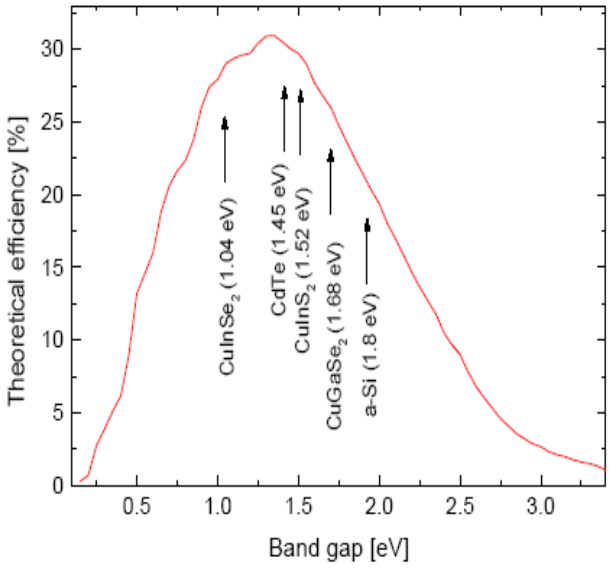


Figure 23 The relationship between theoretical efficiency and energy bandgap (under AM 1.5G).

Due to the deposition process in different condition and method, the CdTe can proceed with the intrinsic doping by both cadmium or tellurium vacancies as crucial defect states. Both important defect state exhibit different electronic behavior in the CdTe film, thus, firstly, the

Cadmium vacancies are shown p-type conductivity for hole density, on the other hand, the tellurium vacancies lead the film to exhibit the n-type conductivity. The most popular deposition techniques for forming polycrystalline CdTe films are sputtering [53], electrodeposition [54], chemical vapor deposition (CVD) [55], vapor transport deposition (VTD) [56], and close-spaced sublimation (CSS) [57][58].

3.5.1 CdTe via Close-Spaced Sublimation (CSS)

The CSS process generally based on the element of reversible dissociation for CdTe under higher source temperature during the fabrication. The process of dissociation for the material express:

$$2CdTe(s) \leftrightarrow 2\ Cd(g) + Te_2(g)$$

which recombine on the substrate surface to form the CdTe film.

The lattice mismatch between the CdS and CdTe is 9.7%, which leads to interface defects that can reduce the photocurrent. The formation of the CdS_xTe_{1-x} layer during the high temperatures utilized by the CSS method improves the quality of the junction by reducing the concentration of recombination centers at the interface. C.S. Ferekides al. has reported the advantage of utilizing the CSS method for deposition of high-quality CdTe film, and the film provides significant large crystalline grain size which indicates a lower defect density and small grain boundary [59]. In the comparison of other methods, the physical vapor deposition and sputtering yields much small grains structure. The incorporation of oxygen-containing ambient allows producing decent crystalline and characteristic properties for CdTe films in different research developments. The presence of oxygen exhibits the better electronic-optical properties of p-type CdTe, and due to the reduction of deposition rate, the grain size remains small which is contributed to creating a high density of the film with reduction of possible pinhole [60].

3.5.2 CdTe via R.F. Sputtering Deposition

The CSS technique has been favored by several groups due to its high deposition rates, relatively large grains, and overall quality of the films. Sputtering has also been a popular process due to its potential for large area deposition. CdTe thin films were grown by R.F. sputtering in an $Ar+N_2$ ambient. Using N_2 partial pressure (~1%) as a substrate temperature at 350 °C with using an R.F. voltage of 1200 V, R.F. power density of about 5 W cm^{-2}, and a bias applied to the substrate of the order of 10% of the R.F. voltage, the resistivity of p-type CdTe film exhibits as low as 9 Ω-cm [61].

3.6 $CdCl_2$ Heat Treatment (HT)

The high efficiency CdTe solar cells required a significant step of the process which is called the $CdCl_2$ heat treatment (HT), it is believed to be an important foundation in the fabrication of devices. $CdCl_2$ treatment is fabricated by the thermal evaporation and numerous methods on the CdTe surface following the post-annealing process under $He+O_2$ ambient. The post-annealing temperatures are in the range of 350 to 400 °C for fixed 25 mins, and it is following by the process of ultra-sonicated clean in methanol to remove residual $CdCl_2$.

The effect of Cl element distribution in the polycrystalline CdTe film has been continuously investigated. The significant effects of $CdCl_2$ treatment have been exhibited with: (a) improvement of the CdS/CdTe interface by promoting inter-diffusion process between CdTe and CdS [62], (b) gain the larger grains size with recrystallization [63], (c) increased carrier collection in the long wavelength [64], and (d) passivation of GBs and deep defects to increase the minority carrier lifetime [65]. The elemental distribution of Cl in the CdTe films exhibited mostly segregated at grain boundaries; thus the only a small portion of Cl (on the order of 10^{16} -10^{17} cm^{-3}) diffusing into the grain interior has been widely investigated [66].

The interdiffusion of S and Te near the CdTe/CdS junction [67] as a result of the $CdCl_2$ HT improves the electronic properties of the CdS/CdTe junction [68] by reducing interface recombination. Figure 24 depicts the before and after device structure with sulfur (S) diffusing into the CdTe layer and creating a $CdTe_{1-x}S_x$ layer (Te-rich alloy), which leads to the reduction of bandgap in CdTe layer and increases carrier collection in the long wavelengths. In addition, the Te diffusion into CdS forms $CdTe_ySe_{1-y}$ (S-rich alloy), which is photo inactive and highly defective.

The presence of oxygen during the $CdCl_2$ treatment improves the performance of the CdS/CdTe solar cell (as compared to using inert ambient), and it is believed to increase the additional p-type hole density due to the formation of shallow-acceptors defects [69]. On the other hand, owing to the passivation of Cl into grain boundary regions, the CdTe become more p-type, which is subjected to increase photo-carrier collection efficiency and lifetime by incorporation of chlorine and oxygen into the GBs [70].

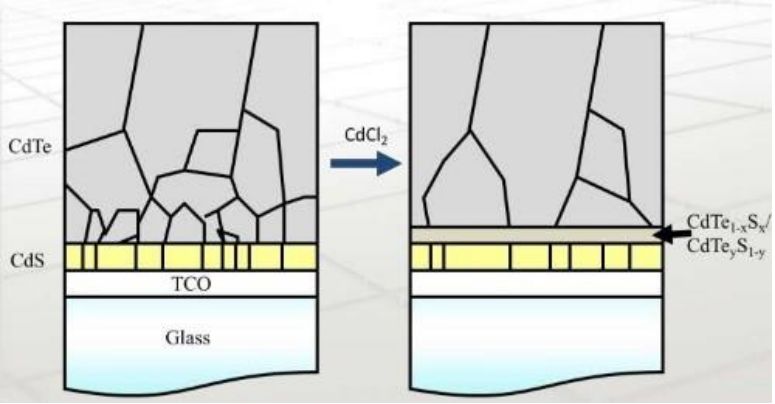


Figure 24 Inter-diffusion of S and Te near the CdTe/CdS junction after $CdCl_2$ HT.

3.7 Back Contact

One of the challenging aspects of the CdTe solar cells forms a decent ohmic contact between p-type CdTe and back contact (BC). The main reason exhibits that the combination of high electron affinity (4.5 eV) and a large band gap (1.45eV) to produce extreme high work

function, which is around 5.8eV. From metal-semiconductor theory, in order to form an ohmic contact at the junction, the work function of the metal must be higher than the work function of the p-type CdTe (5.8 eV). However, it is difficult to find any of the metal materials which match completely the prerequisite. The formation of Schottky barriers junction is exhibited by utilizing the lower work function metal materials (< 5.8eV). The formation of back contact barriers or offset cause the obstacle to transport hole out, and the effect is revealed in the current-voltage characteristics of the solar cell.

Two distinguished methods are designed for forming *"pseudo-ohmic contacts,"* owing to the difficulty in doping p+ polycrystalline CdTe. Firstly, a Te-rich layer is formed by the surface treatment of CdTe for producing a p^+-surface, followed by the deposition of a metallic contacting material. In the second design of process, additional or buffer layer of material has desirable valence band with CdTe, which can be fabricated the pseudo-ohmic contacts. From the research investigation, some of the buffer layers are favorable to dope heavily for p-type at the interface with the metal contact.

3.7.1 CdTe Surface Treatment

The surface treatment for CdTe is prior to the formation of back contact, and the process must be adapted as mentioned above. The two achievements can be accomplished by the surface treatment (etching) of the CdTe surface. The priority of surface treatment is to remove the contamination or oxides from the CdTe surface, which is believed to be formed during the $CdCl_2$ heat treatment. Secondly, it provides a Te-rich film. The surface treatment has been distinguished by each wet or dry chemical etching process based on the use of the medium. According to the dry etching mechanism, it is general methods to utilized for etching processes such as physical

sputtering, reactive ion etching, and plasma etching. Considering the process cost, the wet chemical etching has been popularly utilized for surface treatment in the CdTe surface [71].

The most promising solutions utilized for wet etching, which are Br_2/methanol solutions (BM) [72], aqueous nitric acid/phosphoric acid mixtures (NP) [73] and chromate etches ($K_2Cr_2O_7$:H_2SO_4) [74].

3.7.2 The Role of Copper in the Formation of the Back Contact

The Cu containing back contact is favorably adapted to use for all high efficiency CdTe solar cells. Two possible defects can be formed either a substitutional defect (Cu_{Cd}) or an interstitial defect (Cu_i) by doping Cu into the CdTe layer, respectively. Cu_i is a shallow donor (0.01eV) while Cu_{Cd} is a deeper acceptor level (0.15 - 0.34 eV) [75]. The mobility of interstitial Cu is very high and therefore minimizing the formation of interstitial Cu can minimize transient effects and degradation issues. Although native defects such as V_{Cd} are acceptors, Cu_{Cd} acceptor defects result in higher doping due to their lower activation energy [76]. In order to form the p+ CdTe back contact surface (during the back contact annealing process), the one of acceptor defect (Cu_{Cd}) can achieve this, and due to the p+ channel, it will assist the tunneling effect in establishing an ohmic back between CdTe and BC. The great controlled amount of Cu doping also has been reported for the record-breaking world efficiency on the CdTe thin film devices [77]. As the CdTe layer is over-diffused by Cu back contact after the annealing process, this effect contributes to the instability and degradation of performance in the traditional CdS/CdTe cells. Summary of the defect analysis, the performance has been degraded due to the interstitial Cu (Cu_i), which diffuses fast and easily accumulate at the junction of CdS/CdTe. The study of excessive Cu diffusion cause to compensate for the shallow donor levels with deep acceptors in CdS, and this has been reported by Asher et al. [78]. However, using the suitable amount of Cu diffusion in the interface has been

introduced by the researcher at USF, and also exhibits the presence of Cu on the CdS surface can possibly improve the device performance [79].

3.7.3 Cu Doped Graphite Paste

It is one of the critical methods to achieve the highest conversion efficiency of CdS/CdTe cells, and the Cu doped graphite paste as back contact has been reported [80]. Prior to the fabrication of back contact, the surface treatment of CdTe can form a Te-rich condition in the surface. Cu doped graphite paste is made by a mixture of HgTe: Cu and the contact process followed by low-temperature annealing (250-275 °C) to let the Cu diffusion into the absorber layer. It is suggested that the tunneling effect for ohmic contact can be achieved by the formation of highly p-doped layers of Cu_2Te and $Hg_{1-x}Cd_xTe$ with annealing the Cu doped graphite paste [81].

3.7.4 The Issues of Cu Doped Back Contact

Cu is known to play a significant role in improving the performance of CdTe solar cells. However, Cu is also known to have adverse effects on device performance. Firstly, the uncontrolled Cu doping also causes the reduction of stability in the cells under stress [82]. Secondly, p-type CuCd defect will be compensated by a shallow donor level, which is Cui. It is believed to cause by excessive Cu doping. The higher Cu doping with rapid diffusion into CdTe is also contributed to degrading the performance of the solar cell, due to the deep donor defect for increased recombination centers – i.e., reducing the minority carrier lifetime - and shunt paths at the CdTe/CdS junction. Besides, the enormous back-contact barrier may be formed due to the excess Cu depletion from the back contact that results in the production of a roll-over in the J-V characteristics of the solar cell [83]. The increased thickness of the Cu layer is detrimental for both series and shunt resistances in the J-V measurements; the shunt resistance decreased due to the

shunt paths formed by the excess Cu. Thus, the amount of Cu has to be optimized to achieve the best device performance and stability.

3.8 New Device Architecture: Glass/MZO/CST/CdTe

The performance of thin-film CdTe solar cells has increased significantly during recent years and now exceeds 22 % [1]. Some of the performance improvements were due to the use of $CdSe_xTe_{1-x}$ alloys as absorber layers (CST/CdTe) [84]. The current high efficiency CdTe cell architecture is typical: SnO_2:F/MZO/CST/CdTe/Back electrode, as shown in Figure 25.

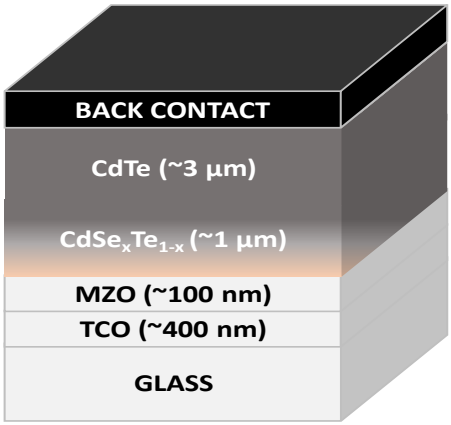


Figure 25 The new configuration of MZO/CST/CdTe for solar cells architecture.

3.8.1 The Magnesium Zinc Oxide (MZO) Layer

The different type of electronic and optical semiconductor devices, including solar cell, laser diodes, and transistor, etc. have been fabricated by the wide energy bandgap of group II-VI semiconductor materials. One of the accessible materials is zinc oxide (ZnO), which has optical near 3.3eV and high transparency. It is known to commonly utilize to apply as a window layer in the thin film solar cells [85]. The wide band gap (3.3 eV) and an enormous excitation binding energy (60 mV) of ZnO heterostructure devices, synthesis of ternary $Mg_xZn_{1-x}O$ alloys has been reported, which has the band gap wider than ZnO [86]. $Mg_xZn_{1-x}O$ films are considered as a promising material for several optical applications due to its high excitation binding energy and wide tunable band gap [87]. Due to these added advantages, $Mg_xZn_{1-x}O$ is suggested to be a

promising material for the production of PV technologies and has been massively investigated. In recent studies, incorporation of various Mg compositions with ZnO can tune the location of the conduction band and modify the bandgap alignment with p-type semiconductors, especially in CdTe based solar cells [88]. Also, due to the optimization of band alignment as *"spike"* between $Mg_xZn_{1-x}O$ and CdTe is proven to decrease the interfacial recombination velocity for improving the minority carrier lifetime. Various Mg compositions can synthesize the $Mg_xZn_{1-x}O$ layers which are generally deposited by using R.F. co-sputtering at room temperature. The fabrication of MZO offers very flexibly and controllable in compositions. A possibility of preparing an $Mg_xZn_{1-x}O$ film of the required features may provide the idea to improve the performance of optoelectronic devices.

3.8.2 The Cadmium Selenium Telluride (CST) Layer

Geisthardt et al. are shown the potential characterization in CdTe technology, which can be used to analyze the performance limit in the real experimental condition [89]. The numerous simulations have been reflected that the reduction of bandgap in CdTe materials from 1.45 to 1.36eV, the photo-current would be generated enormously and suggested to compensate for the degradation of voltage that results in increasing efficiency. In order to reduce the bandgap of CdTe to 1.36eV [90], the incorporation of selenium can produce the various Se composition of $CdSe_xTe_{1-x}$ alloys, which is followed by the bowing effect [91]. Paudel and Yan et al. exhibited that the CST alloys can be fabricated in the process of inter-diffusion between CdSe, which is deposited by sputtering and CdTe layer during the $CdCl_2$ post-annealing process [92]. The formation of CST alloys based on the reduction of bandgap, which resulted in the increased current collection in the long wavelengths. The inter-diffusion process can control the amount of selenium alloying with CdTe that was dependent on the thicknesses of CdSe. Due to the bandgap of CdSe (1.7eV), the

residual CdSe believes in producing poor cell performance, and the window loss in the carrier collection, thus it is important to fully diffuse the sputtered CdSe layer into CdTe to form CST alloys. However, this fabrication process shows that the CST alloys are difficult to form a uniform and homogeneous single bandgap below 1.45eV. On the other hand, the new method exhibited that the single deposition of CdSeTe alloys can be well controllable over the selenium alloying. As-deposited single bandgap CdSeTe alloys have been characterized to analyze the effect of selenium composition on the new CdTe device. Finally, the single bandgap CdSeTe alloy will be deposited at the front of a CdTe cell to assess increased current collection at longer wavelengths similar to the sputtered CdSe method [93].

CHAPTER 4

EXPERIMENTAL MEASUREMENT AND PROCESS

4.1 Device Measurement

In semiconductor research, materials are characterized by multiple techniques to analyze the morphology, topography, electrical, and optical properties in order to understand their impact on devices. Understanding the importance of material properties and their impact on device performance is critical in improving device operation, and in the case of solar cells conversion efficiency. In this work, the techniques described below were utilized for characterizing material and device properties.

4.1.1 X-Ray Diffraction (XRD)

X-ray powder diffraction (XRD) is the most common characteristic technique primarily utilized for identifying the phase of a crystalline material and can provide analytical information on unit crystal cell dimensions [94]. The XRD data which show relatively crystalline orientation peaks over as 2θ range of 20–80° were collected using a Rigaku X-ray diffractometer with CuKα radiation of wavelength 1.54056 Å. The following Bragg diffraction equation calculates the orientation peaks:

$$2d\sin\theta = n\lambda \qquad (14)$$

where n is a positive integer and λ is the wavelength of the incident wave. For a crystalline solid, the waves are scattered from lattice planes separated by the interplanar distance d:

$$d = \frac{a}{\sqrt{h^2 + k^2 + \ell^2}} \qquad (15)$$

where a is the lattice spacing of the cubic crystal, and h, k, and ℓ are the Miller indices of the Bragg plane.

XRD was used to study as-deposited and annealed films to understand the effect of heat treatments. It was also used to calculate the composition of ternary alloys, such as MZO and CST by calculating the lattice constant.

4.1.2 Scanning Electron Microscopy (SEM)

Scanning electron microscope (SEM) is a type of electron microscope with beam energy around 20-30k eV that generates images of a sample via scanning the surface with a focused electron beam. The electrons interact with atoms in the sample, offering various signals that provide information about the surface topography and composition of the elements [95]. For this study, a Hitachi 800, etc. were used.

SEM was used to understand the growth dynamics of the CST CSS deposition, understand the extent of grain growth during the $CdCl_2$ HT, etc.

4.1.3 Transmission Electron Microscopy (TEM)

In this dissertation, MZO/CST/CdTe solar cells were utilized the High-Resolution Transmission Electron Microscopy (HRTEM) to characterize the cross-section materials structure. Prior to the TEM measurement, the samples require the preparation of Focused Ion Beam (FIB) milling by using a dual beam FEI Nova 600 Nanolab. A standard in-situ lift-out process was utilized to make the cross-section samples through the film bulk into the glass substrate. A platinum overlay was deposited on the top of the film to define the area of interest on the surface of the sample, homogenize the final thinning of the samples and to prevent damage to the CST or CdTe film surface from the ion beam. STEM bright-field images and high-resolution TEM images were collected using an FEI Tecnai F20 (S) TEM operating at 200 kV [96].

The TEM cross-section images are shown both of CdSe/CdTe and CST/CdTe solar cells structures and lead to understanding the grain structure and element distribution of the cell devices.

4.1.4 Time-Resolved Photoluminescence (TRPL)

The time-resolved photoluminescence (TRPL) was also utilized to characterize recombination in thin films of CdTe and/or CST and determine an effective minority carrier lifetime. Time-Resolved Photoluminescence (TRPL) was obtained with excitation at 640 nm with 0.3 ps pulses at 1.1 MHz, and PL was measured with 10nm bandpass filter with the center at 820 nm. TRPL is a contactless method to characterize recombination and transport in photovoltaic materials. The strengths and weaknesses of the technique have been described elsewhere [97].

For this work, the study of MZO as a window layer and CST as absorber layer are significant to increase the minority carrier lifetime due to the improvement of the recombination center. Thus, the TRPL data are defined as the lifetime in the various excitation energies on the cells.

4.1.5 Capacitance-Voltage Profiling

The C-V catheterization technique is the most common electric measurement of the depletion region capacitance of semiconductor junctions including p-n junctions, metal-semiconductor junctions, and metal-oxide-semiconductor (MOS) structures without damaging the samples, in comparison of other semiconductor profiling techniques such as Hall effect, SIMS, etc. The rapid analysis and non-destructive character define the C-V measurement with excellent usage in the semiconductor industry. The C-V (capacitance versus voltage) measurement provides the method to calculate the doping profile of semiconductor devices, which is done using an asymmetric semiconductor junction [98]. The CV measurements were performed using an HP 4194A impedance/gain-phase analyzer.

CdTe and CST solar cells were characterized using CV to understand the effect of Se composition Cu annealing temperature etc. on the net doping in the absorber films.

4.1.6 I-V Measurement

I-V measurements are essential in characterizing junctions such as solar cells. When performed under light, one can obtain the four important output parameters of the solar cell, V_{OC}, J_{SC}, FF, and efficiency. Calibrated *Solar Simulators* are used to simulate the solar spectrum; depending on the optics and light sources, various air mass conditions can be simulated, including AM1.5G, which is used for characterizing solar cells for terrestrial applications. Dark IV measurements can be used to evaluate the quality of the junctions/solar cells by extract in parameters such as diode factors, reverse saturation currents series and shunt resistances, etc.

A four-point probe set up to mitigate contact resistance was used with a Keithley 2410 Source meter, and the current output was measured as the voltage bias was swept. The data was collected using a LabVIEW program, and the V_{OC} and FF of the devices were calculated. In addition, I-V measurement is simulated by WxAMPS software for the different type of superstructure configuration devices as well.

4.1.7 Spectral Response

The spectral response (SR) of the solar cells was measured using an Oriel monochromator (model 74100). A GE400w/120v Quartz Line lamp (model 43707) was used as a light source. The light intensity was measured using a reference silicon solar cell calibrated by the National Renewable Energy Laboratory (NREL). The following equation calculates the quantum efficiency:

$$QE_{Sample} = \frac{I_{Device}}{I_{Reference}} QE_{Reference} \qquad (16)$$

SR data and the AM1.5G standard tables were used to calculate the J_{SC} of solar cells.

4.1.8 Deep Level Transient Spectroscopy (DLTS)

DLTS measurements were characterized with a Sula Technologies Deep Level Spectrometer. The sample temperature was changed from 120 K to 300 K using liquid N_2 and a heater inside a Janis VPF-100 cryostat. The DLTS measurements were conducted under a bias pulse of -1 to 0 V with a pulse width of 1ms. The resulting capacitance transients were analyzed with 6 different rate windows from 0.02 to 1 ms. During the DLTS measurement, the capacitance transient of a reverse biased p+n or n+p junction due to charge carrier injection is measured. The following equation gives the capacitance transient,

$$C(t) = C_0\left[1 - \frac{N_T}{2N_D} exp\left(-\frac{t}{\tau}\right)\right] \quad (17)$$

where C(t) is the instantaneous capacitance, C_0 is the reverse bias background capacitance, N_T is the trap concentration, N_D is the doping concentration, and τ is the carrier lifetime [99].

4.2 Experimental Process

The MZO/CST/CdTe cells discussed in this paper are of the superstrate configuration and were fabricated on Corning EagleXG glass. ITO was deposited by sputtering, and its sheet resistance was approx. ~ 8 Ω/□. MZO was also deposited by sputtering was used as the emitter layer. Following the deposition of MZO, a CdS layer was deposited by CSS with thickness in the range of 100-200 Å. The CST alloys were deposited to approx. 1 µm thickness, followed by CdTe also by CSS to a thickness of 3-4 µm. After the CdTe deposition, the devices were $CdCl_2$ heat treated. The $CdCl_2$ HT was carried out on $He:O_2$ ambient at temperatures in the range of 410 – 440 °C. Prior to the formation of the back contact, the CdTe surface was etched in a bromine-methanol solution. The back contact was Cu-doped graphite.

4.2.1 $Mg_xZn_{1-x}O$ by Co-R.F. Sputtering

The $Mg_xZn_{1-x}O$ thin films were formed by using the RF co-sputtering with ZnO (99.99 %) and MgO (99.99 %) targets simultaneously. In the sputtering system, each of the targets was the diameter of 3 inches and had been set up in a distance of around 25cm far from the substrate during the deposition. The substrate was rotated during the sputtering to enhance the uniformity of MZO film and was performed at room temperature and various partial pressure $Ar+O_2$. From Table 4.1, the Mg compositions of MZO are defined by the varied sputtering powers applied to each target to control the deposition rate, and ZnO and MgO targets were conducted sputtering simultaneously by opening the shutters. The applied sputtering power to each target was different formation 0 to 180 W. The $Mg_xZn_{1-x}O$ films ($0 \leqq x \leqq 0.5$) were deposited on fused glass substrates at room temperature in 5 X 10^{-3} torr of 10 % oxygen mixed with Argon [100]. The chemical composition ratios of $Mg_xZn_{1-x}O$ were determined by Energy Dispersive X-ray Spectroscopy (EDS). The phase and crystallographic structure were characterized by X-ray diffraction (XRD) operated at 45 kV and 40mA using Cu Kα radiation. The optical transmission was recorded on a sphere scanning spectrometer at a wavelength from 400 to 1200 nm. The band gap energies were derived from a plot of $(\alpha h\nu)^2$ as a function of photon energy ($h\nu$). The resistivity was measured using the four-point probes measurement.

Table 4.1 Sputtering power of MgO and ZnO respectively by using RF co-sputtering.

Mg compositions	MgO power (W)	ZnO Power (W)
0	0	100
0.15	110	100
0.23	120	100
0.3	135	100
0.4	160	100
0.5	180	100

4.2.2 Formation of $CdSe_xTe_{1-x}$ by Inter-Diffusion

CdSe has been recently used for the fabrication of $CdSe_xTe_{1-x}$ alloy-based cells to improve carrier concentration and lifetime [101]. Compared to S, Se has a higher solubility in CdTe, allowing for higher Se concentrations in $CdSe_xTe_{1-x}$ and therefore, lower bandgap [102]. The effective bandgap of $CdSe_xTe_{1-x}$ depends on the amount of Se in the alloy. There exists an optimum amount of Se, for which the bandgap reaches a minimum due to the bowing band effect before it starts increasing again. One of the most critical steps to achieve high efficiency CdTe solar cells is the $CdCl_2$ HT. This treatment improves p-type doping, enhances carrier collection, causes recrystallization, and promotes inter-diffusion of at the CdS/CdTe junction, which reduces interface recombination [103]. The $CdCl_2$ annealing temperature and time can be used to control the CdSe/CdTe inter-diffusion. Another critical parameter is the CdSe thickness since any unused CdSe layer can be detrimental to the device performance as it lowers V_{OC} [104]. The effect of CdSe thickness and $CdCl_2$ HT on the CdSe/CdTe inter-diffusion and the photovoltaic device performance is presented in this work.CdSe was deposited by RF sputtering in Ar ambient at room temperature. CdSe thicknesses were varied between 75 – 1500 Å. CdS and CdTe were deposited by close-spaced sublimation (CSS). After the CdTe deposition, the devices were $CdCl_2$ heat treated, which is a standard processing step for CdTe solar cells. The $CdCl_2$ HT was carried out under He: O_2 ambient at temperatures ranging 390 – 450 °C. Prior to the formation of the back contact, the CdTe surface was etched in a bromine-methanol solution. The back contact was Cu-doped graphite, followed by thermal annealing.

4.2.3 Formation of $CdSe_xTe_{1-x}$ via Direct CSS

This work describes the properties of $CdSe_xTe_{1-x}$ (CST) alloy films and solar cells produced by the Close-Spaced sublimation (CSS). The source materials were CST alloys of various

Selenium compositions (x=5, 10, 15, 20, and 25 %). Solar cells had the configuration: TCO/$Mg_yZn_{1-y}O$ (MZO)/CST/CdTe. The properties of CST films and cells were investigated as a function of Se composition (x), substrate temperature (T_{SUB}), and ambient used during the CSS deposition, which is shown in Figure 26. It was found that increasing the Se composition resulted in smaller grain sizes and lower open circuit voltage (V_{OC}) corresponding to the reduction in band gap with increasing Se composition. The grain size was also found to increase with increasing substrate temperature (550 – 640 °C) from 1 to 3 µm. Capacitance measurements indicated a small but consistent increase in net p-type doping with increasing substrate temperature, which was accompanied by an increase in V_{OC}. The addition of oxygen during the CSS deposition resulted in improved film density. The CST films were deposited by CSS using in-house synthesized CST sources prepared from CdTe (99.999 %) and CdSe (99.999 %) powders. The Se composition of the CST sources and films was measured using Energy Dispersive X-Ray Spectroscopy (EDS), and it depended on the source sublimation temperatures as shown in Figure 27.

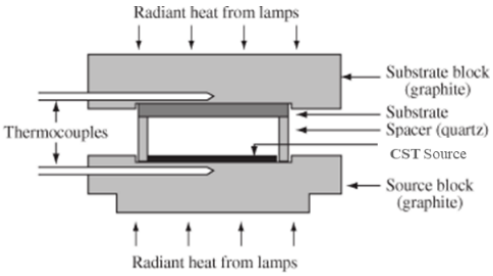


Figure 26 The Close Spaced Sublimation system for depositing the CdTe and CST alloy.

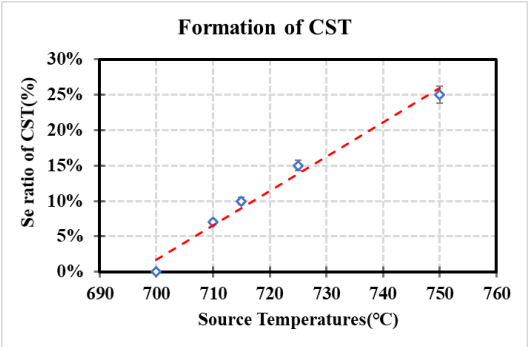


Figure 27 Formation of CST films by Close Spaced Sublimation (CSS) with different source temperatures.

CHAPTER 5

STUDY OF WINDOW LAYER

Figure 28 shows the substrate configuration of the CdTe cell investigated during this project. The ternary compound MZO has been recently used as a window layer to replace CdS [105]. Its larger bandgap allows for additional J_{SC} gains in the short wavelength range of the solar spectrum, below 510 nm, the absorption edge for CdS. As indicated in Chapter 4.2.1 the composition of MZO is an important material property that influences its bandgap, conductivity, and conduction and valence band location, among others and therefore it must be optimized for the CdTe solar cell for maximum performance.

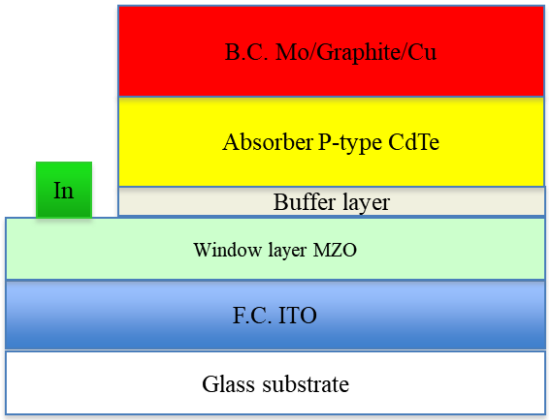


Figure 28 Application of $Mg_xZn_{1-x}O$ as a window layer on the CdTe thin film solar cells.

5.1 Characterization of $Mg_xZn_{1-x}O$

$Mg_xZn_{1-x}O$ films with several composition ratios were prepared by RF magnetron co-sputtering of ZnO and MgO targets. Table 4.1 shows the Mg content of these films determined by EDS measurements and the sputtering power applied to ZnO and MgO targets, respectively. The

Mg composition increased as the ratio of the ration of the MgO to ZnO sputtering power applied to the target increased.

As-deposited (at room temperature) $Mg_xZn_{1-x}O$ was found to be amorphous; thus, the XRD measurement was unable to detect the XRD patterns. Figure 29 shows XRD patterns of $Mg_xZn_{1-x}O$ films, which were annealed at 400 ℃ in inert ambient (He) for 20 minutes. A single peak corresponding to the (002) direction of the wurtzite hexagonal structure is present; this is consistent with previous work that demonstrated the structure for compositions below 0.50 [106]. The basic structure of $Mg_xZn_{1-x}O$ remains the same as that of ZnO for $x<0.50$. As the Mg content increased, the (002) peaks shifted to higher diffraction angles. This shift suggests that the spacing of the plane narrows as the Mg content increase.

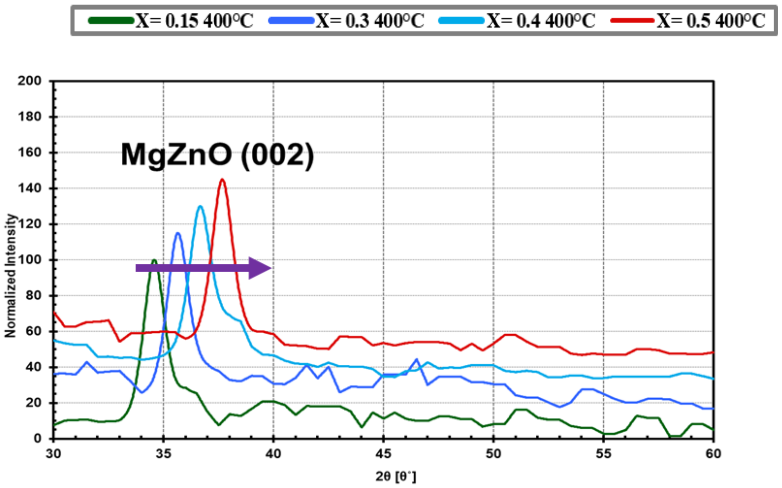


Figure 29 XRD patterns of $Mg_xZn_{1-x}O$ films [$0.15 \leqq x \leqq 0.5$] grown on glass substrates and annealed at 400˚C in He ambient gas.

Figure 30 shows the transmittance spectra for the films shown in Figure 29. The transmittances of all $Mg_xZn_{1-x}O$ films were greater than 80%. A gradual shift of the absorption edge towards shorter wavelength with increasing Mg content is observed, as should be expected due to an increase in the energy gap. These data were used to calculate the absorption coefficient using the equation shown below

$$\alpha h\nu = C\,(h\nu - Eg)^{1/2} \qquad (18)$$

where hν is the photon energy, Eg is the optical band gap, and C is the characteristic parameter of the transitions. The optical band gap was evaluated by extrapolating the linear portion of the $(\alpha h\nu)^2$ versus hν plot onto the energy axis. The variation of the energy band gap as a function of Mg-content is shown in Figure 31. The band gap increased almost linearly from 3.3 eV to 4.2 eV; this is in good agreement with what Kephart et. Al. obtained previously [107].

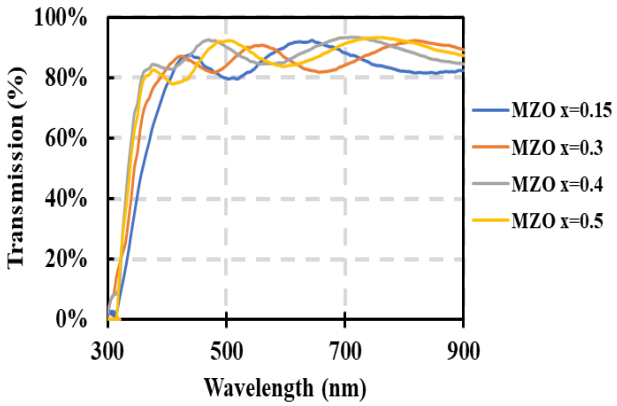


Figure 30 Transmission spectra of $Mg_xZn_{1-x}O$ films with various Mg compositions.

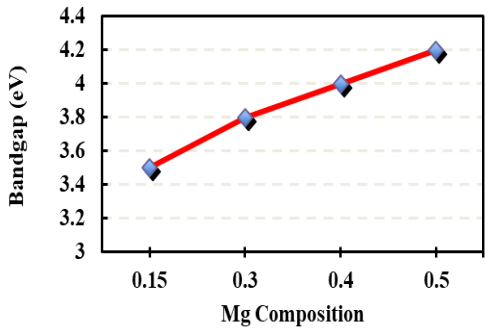


Figure 31 Optical bandgap of $Mg_xZn_{1-x}O$ films with various Mg compositions.

Figure 32 shows the variation of resistivity as a function of Mg content. Resistivities of as-deposited films with higher Mg content was significantly higher and exceeded 10^7 (Ω-cm). Annealing in inert of oxygen ambient @ 500C resulted in lower resistivity in all instances. The trend of increasing resistivity with Mg content remained. The mechanism for the lower resistivity is not understood at this time and was not investigated further. It is possible that annealing

improves mobility due to improvements in crystallinity since as-deposited films were amorphous and became polycrystalline after annealing.

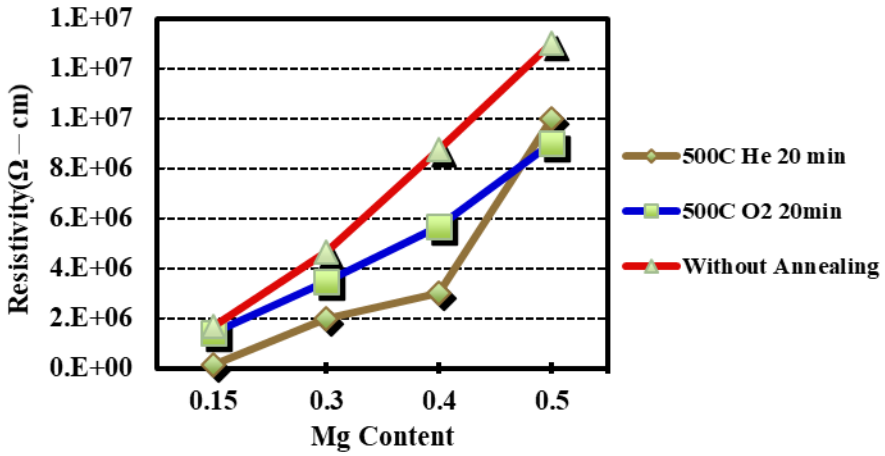


Figure 32 The resistivity of $Mg_xZn_{1-x}O$ films as a function of Mg contents with different post-annealing conditions.

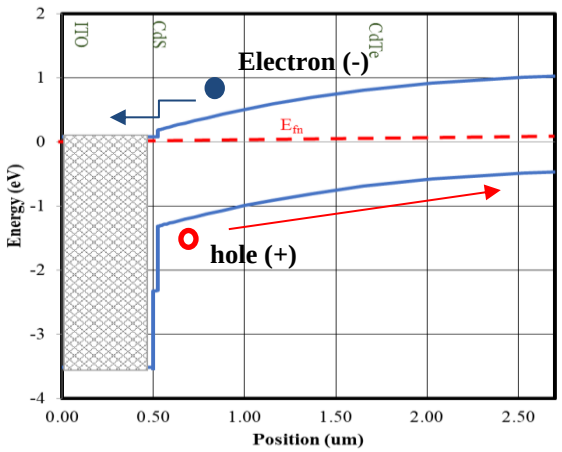


Figure 33 A basic energy band diagram of p-type CdTe devices and the light should be transmitted to the absorber, and charge carriers should be transported out.

5.2 MZO/CdTe Interfacial Band Alignment – Modeling Results

Figure 33 shows the energy band diagram of an ITO/CdS/CdTe device and Figure 34 shows several ITO/MZO/CdTe energy band diagrams for three different MZO bandgaps (i.e., three different MZO compositions). If the conduction band of the window is lower than that of the absorber, the resulting energy offset will result in a reduction in V_{OC} and fill factor by encouraging interface recombination. A similar situation can occur if the window is degenerately doped. The

Fermi level of the degenerately doped material can be leveled with the absorber conduction band, but typically accumulation in the semiconductor will not occur because the Fermi level is pinned at the conduction band of the absorber. Since the Fermi level is above the conduction band minimum of the highly doped layer, the window CBM will now be below the absorber CBM are displayed in Figure 34 (a). In the other case, if the conduction band of the window layer is above the conduction band of the absorber, there will be a barrier that the electron must surmount in order to be collected. This is referred to as a *"spike."* If this spike is small, on the order of ~ 0.3 eV, it will not limit device performance, but if too high CBO ~ 0.8 eV, a barrier to current flow or *"kink"* will form. The latter is depicted in Figure 34 (c). The approximate maximum height is calculated by setting the saturation current of a Schottky barrier to the photocurrent and is approximately 0.3 eV for typical materials [108]. Therefore, the ideal electronic material for a window layer is non-degenerately doped and has a flat or small conduction band spike. Optically, the window layer should absorb as little light as possible (ideally zero), which means that a higher bandgap material and a thinner layer is desired. The impact of the emitter/absorber interface on CdTe cell performance results from (1) the conduction-band offset ΔEc, (2) the emitter doping and thickness, and (3) the density and energy distribution of interface defects. A positive ΔEc (spike) is beneficial to cell performance, which is shown in Figure 35 (modeling by WxAMPS) since it can induce a substantial hole barrier that suppresses the interface recombination [109].

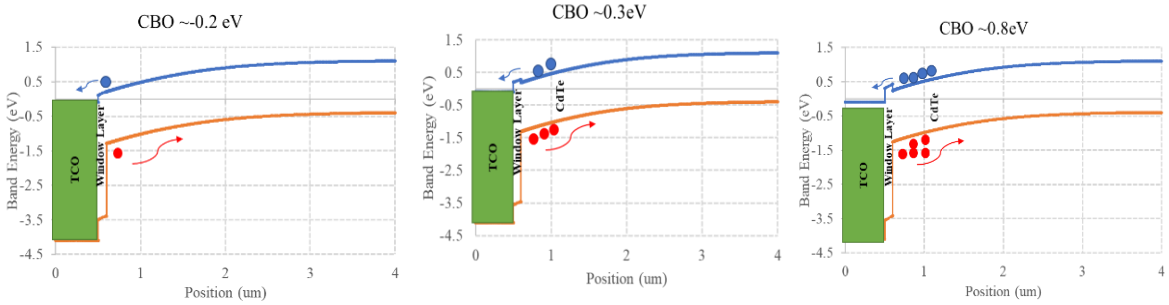


Figure 34 (a) Refer as a cliff (b) a flat or small spike (c) a large positive CBO as big spike will present a secondary barrier to electron flow by AMPS modeling.

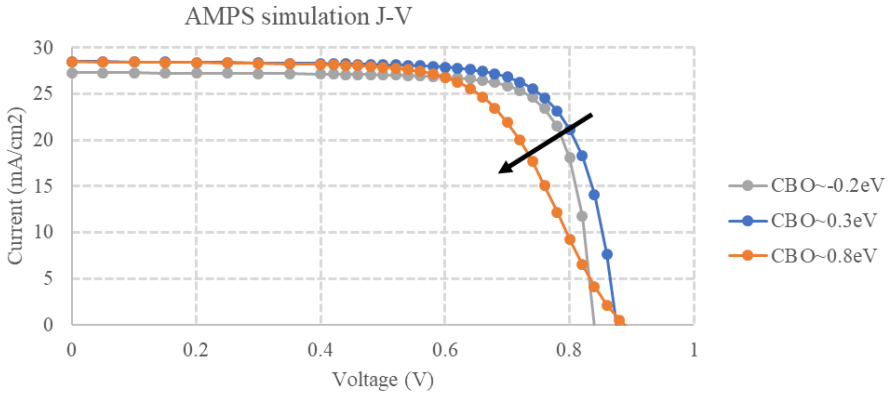


Figure 35 The J-V curves of the devices with the various CBO (-0.2 to 0.8 eV) are simulated by WxAMPS.

5.3 The Effect of MZO Bandgap on the Devices

Band alignment measurements have indicated that a ZnO/CdTe junction results in a negative conduction band offset. ZnO alloying with MgO to produce $Mg_xZn_{1-x}O$ can shift the location of the conduction band of MZO to lower the offset or produce a small spike at the MZO/CdTe interface. Increasing the composition also adds the benefit of increasing the optical bandgap of the layer for better UV light transmission so that the photon current can be generated in the high-energy spectrum region (short wavelengths).

In order to understand the effect of both CdS and MZO thicknesses, CdS buffer layer were deposited between MZO and CdTe with various thicknesses of CdS film layer (deposition times 0 to 80 sec), which were deposited by the Close Space Sublimation deposition. Thus, the devices of summary performances are demonstrated thicknesses of MZO (x=0.3) between 25 - 400nm is shown in Figure 36. The thicker MZO layer (> 1500 Å), is believed to cause an S-kink or roll-over in the current-voltage curve, regardless of MZO compositions are defined as functions as a window layer as the band alignment of the structure has been preliminarily optimized. However, MZO layers thinner than 100 nm show reduced Voc. It is believed to be associated with the increased electron barrier in the conduction band as devices have thicker MZO layer. On the effect of CdS,

the thicker CdS can result in better FF, but the J_{SC} shows a significant loss due to the window loss in the short wavelength.

Results on MZO/CdTe resulted in JV with a significant rollover regardless of the MZO composition. It was also observed that the performance was not very reproducible. This behavior was attributed to the quality of the MZO/CdTe interface and potential instability of the MZO when exposed to the conditions of the CSS CdTe deposition process. In order to test this hypothesis, subsequent experiments incorporated a very thin CdS layer between MZO and CdTe: MZO/CdS/CdTe. The thickness of CdS was approximately 25-50 nm. Spectral response measurements of MZO/CdS/CdTe junctions (with MZO compositions from 0 to 0.35) are shown in Figure 37. The corresponding bandgap is greater than 3.3 eV (the bandgap of ZnO), and therefore no losses are observed in the short wavelength range.

Figure 38 is shown all the devices of JV which exhibit V_{OC} approached up 840 mV as the MZO composition x > 0.23; The window layers with higher magnesium compositions produce an extreme kink in the J-V curve due to the larger conduction band offset. Therefore, at the optimal thickness of 100 nm, made with the x=0.23 magnesium composition, numerous devices with efficiency values are revealed the performance over 15% in Table 5.1.

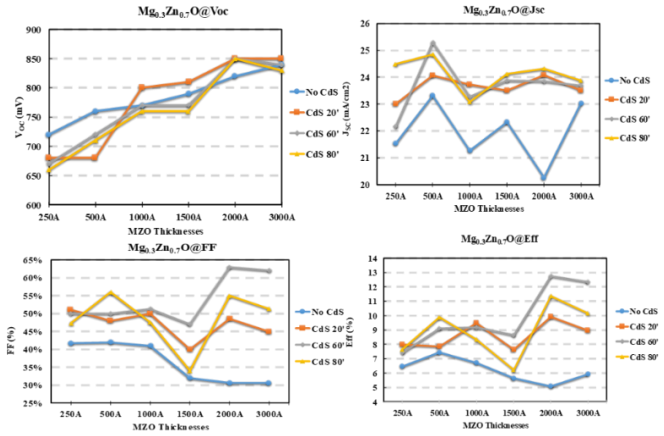


Figure 36 The performances summary with $Mg_{0.3}Zn_{0.7}O$ (250 to 3000 Å) as window layers in various CdS deposition time (0 to 80 s).

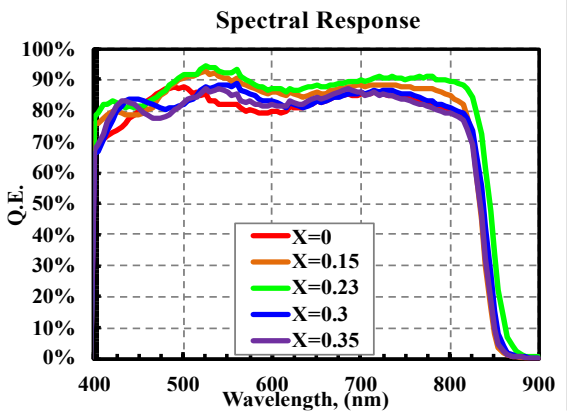


Figure 37 The spectral response shows the Mg compositions from 0 to 0.35 in the wavelength between 400 to 900 nm.

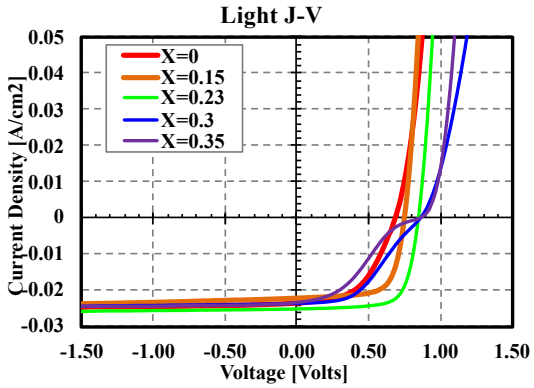


Figure 38 The J-V curves of the devices with the MZO thickness of 100 nm on the compositions from 0 to 0.35.

Table 5.1 Summary table of $Mg_xZn_{1-x}O$ (x=0 to 0.35) devices.

$Mg_xZn_{1-x}O$	V_{OC} (mV)	FF (%)	J_{SC} (mA/cm^2)	Efficiency (%)
x=0	680	51.10%	23.01	7.99
x=0.15	760	70.00%	24.07	12.81
x=0.23	840	72.00%	25.29	15.30
x=0.3	850	46.00%	23.47	9.18
x=0.35	860	33.00%	23.05	6.54

5.4 The $CdCl_2$ Effect on MZO/CdTe Devices

The $CdCl_2$ effect has been an essential processing step for CdTe cells since the late ’80s. Cells fabricated with MZO as the window layer were $CdCl_2$ heat treated under various conditions

to understand whether this process needs to be re-optimized for the new window, and the JV and SR are shown in Figure 39. The optimum $CdCl_2$ heated treatment temperature for typical USF CdS/CdTe devices has been 390 °C [110]. For MZO/CdTe devices, a higher temperature of 410 °C was found to be optimum, as shown in Table 5.2. Temperatures above 390 °C were most likely causing excessive interdiffusion for the CdS/CdTe junction resulting in lower performance; other studies have also indicated loss of adhesion and delamination [111]. It appears that the MZO/CdTe interface can tolerate higher annealing temperatures. The improved performance for MZO/CdTe junctions at the higher $CdCl_2$ annealing temperature, suggests that the chlorine passivating effects are more effective at higher temperatures. This could suggest (a) either enhanced recrystallization – i.e., larger grains and smaller GB volume – and/or (b) increased Cl concentration in the GB is needed for better GB passivation. At 430 °C MZO/CdTe performance appears to degrade; this could be related to excessive amounts of Cl reaching the MZO/CdTe interface as the initial stages of a rollover begin to appear in the J-V data. The spectral response shows the carrier collection improve near the absorption edge with increasing $CdCl_2$ HT temperature, and it is associated with the minority carrier lifetime increasing at higher $CdCl_2$ temperatures. The best $CdCl_2$ HT temperature has been optimized at the 410 °C with efficiency approx. 15%.

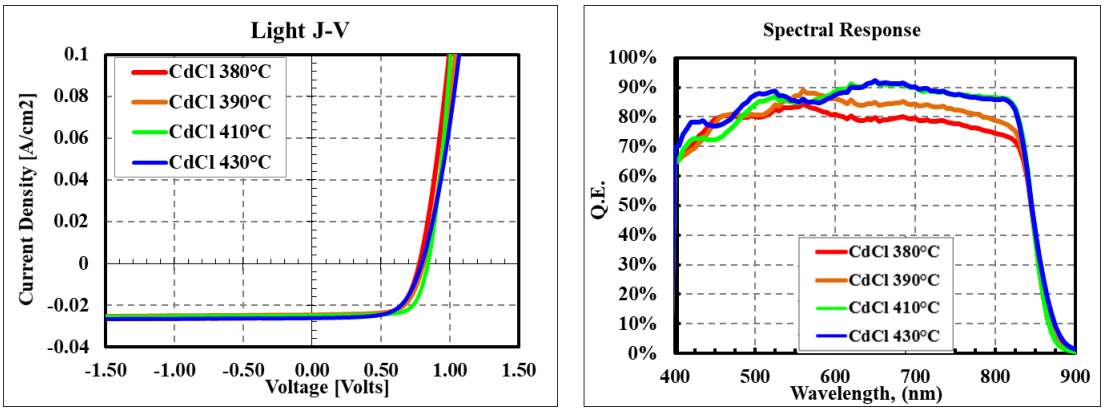


Figure 39 (left) JV and (right) SR data for devices $CdCl_2$ treated at 380 to 430°C with MZO (x=0.23)/CdTe devices.

Table 5.2 Summary table of $Mg_xZn_{1-x}O$ (x=0.23) devices in various $CdCl_2$ HT temperature.

$CdCl_2$ HT	V_{OC} (mV)	FF (%)	J_{SC} (mA/cm^2)	Efficiency (%)
380°C	790	67	24.59	13.02
390°C	800	68	24.59	13.38
410°C	830	72	25.33	15.64
430°C	800	70	24.92	13.96

5.5 Instability of MZO in Interface

$Mg_xZn_{1-x}O$ (MZO) has clearly demonstrated to be a suitable replacement for CdS. The devices are no CdS as a window layer that it is believed to penetrate more light into the absorber, and the MZO bandgap and electron density can be tuned based on the Mg of compositions, thus yielding the optimum conduction band offsets and adjusting recombination rates between TCO/MZO and MZO/CdTe interfaces can be accomplished. However, when the MZO as window layer was employed in the CdTe thin film solar cells, the effect of Mg composition and MZO materials itself has remained to complicate and challenging due to the lack of reproducibility and abnormal (roll-over) current-voltage curves. Simulations (WxAmps) indicate that this anomalous behavior can be attributed to front interface barrier effects. Recent experiments demonstrated that this common MZO interface problem could be resolved experimentally by surface preparation, pre-heat steps, and removing oxygen during absorber deposition and $CdCl_2$ treatment [112]. Oxygen during the cell fabrication process is likely to alter the MZO surface properties and MZO/CdTe band alignment. Two approaches can avoid this effect of oxygen. Firstly, after the deposition of MZO, the samples are performed in the higher temperatures with post-annealing treatment to stabilize the materials. Secondly, The fabrication process has been modified with no-oxygen as ambient in any of deposition, including CSS CdTe, and $CdCl_2$ HT treatment, etc. During

this work, oxygen was not eliminated from the fabrication process; an additional annealing step was developed to improve the MZO surface, which allowed for efficient solar cell fabrication. Prior to the deposition of CdTe, the MZO films were annealed in the presence of CdS vapors. A CdS and the MZO/Glass substrate held in close proximity were heated at high temperatures (580-640C); the experimental set up is shown in Figure 40. EDS analysis after this annealing step did not detect Cd or S on the surface of MZO.

Figure 41 illustrates a strong roll-under *("kink")* in the fourth quadrant of the J–V characteristic that was observed for all the devices exposed to the CdS vapors. This roll-under reduces the FF of all the cells to less than 50 %, thereby severely limiting device efficiency. Devices made with MZO composition of 0.23 reached 870–890mV Voc; the FF remained relatively low. Annealing the MZO films in inert of H_2 ambient did not have the same effect as the CdS vapor annealing process, i.e., the roll-over did not improve.

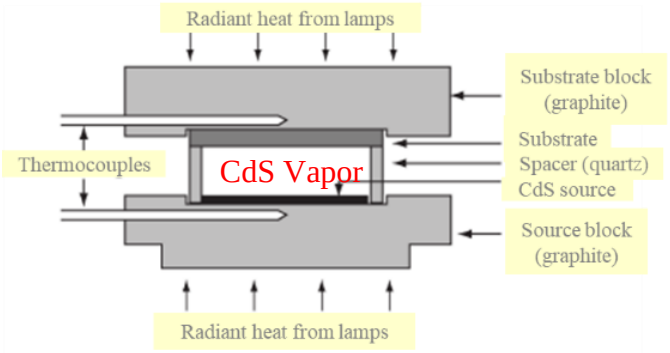


Figure 40 The diagram of Close Spaced Sublimation system with the process of CdS vapor for MZO films.

In summary, the MZO/CdTe thin film solar cells have been fabricated with additional CSS CdS vapor annealed process in varied temperatures. The performance of devices (V_{OC}, FF, Eff) are shown in Figure 42. Due to the stability improvement of MZO, the J-V measurement is no sign of roll-over so that the FF is increased considerably compared with the MZO devices has not been CdS vapor annealing. The V_{OC} is still retaining the high level of performance, owing to the effect

of interfacial band alignment. Therefore, with the elimination of S-kink, the best performing MZO/CdTe cell has accomplished an efficiency up to 15 % with a V_{OC} of 0.860 V and FF of 65% shown in Figure 42 as well. The results provide significant insights for improving the performance of MZO/CdTe solar cells.

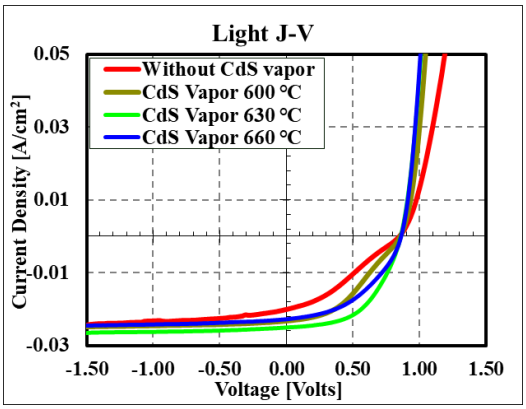


Figure 41 The light J-V in the various CdS vapor temperatures on the MZO devices.

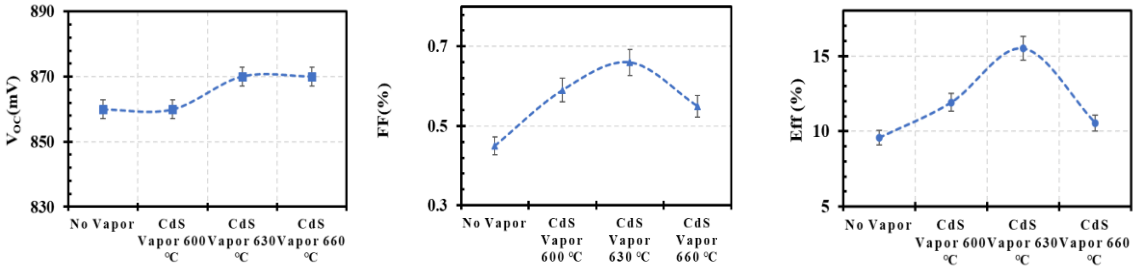


Figure 42 The performances summary are shown for devices made with $Mg_{0.23}Zn_{0.77}O$ as window layers devices in various CdS vapor temperatures process.

CHAPTER 6

STUDY OF BI-LAYER CDSE/CDTE

The highest efficiencies of thin-film CdTe solar cells have increased drastically during recent years and now exceed 22.1% [1]. The limitation in performance for polycrystalline CdTe cells has been primarily due to their low carrier concentrations and lifetimes. One of the innovations was the alloying of CdTe with CdSe that resulted in a lower bandgap absorber and therefore higher J_{SC}. Cells discussed in this chapter were fabricated via the interdiffusion of CdSe/CdTe bi-layers to form CST. The configuration of the device is ITO/MZO/CdS/CdSe/CdTe/Cu-doped graphite (Figure 43).

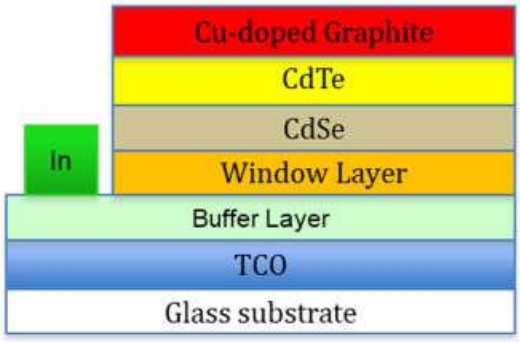


Figure 43 Configuration of CdSe/CdTe solar cells.

6.1 J_{SC} in Inter-Diffusion Bi-Layer CdSe/CdTe

Figure 44 shows SR data and the corresponding to several devices fabricated by interdiffusion of CdSe and CdTe using various CdSe thicknesses. The SR in the 400-820 nm range begins to decrease when the thickness of CdSe exceeds 300 nm. This is believed to be due to incomplete interdiffusion that results in a CdSe/CST/CdTe structure. In order to evaluate the impact of CST formation on the "gains" in J_{SC} due to the smaller CST bandgap, the current

generation above 830 nm was calculated by integrating the SR with AM1.5G. These data are shown in the plot below the SR chart and suggests that at the largest thicknesses the gains are higher, due to the formation of a CST with the smallest bandgap.

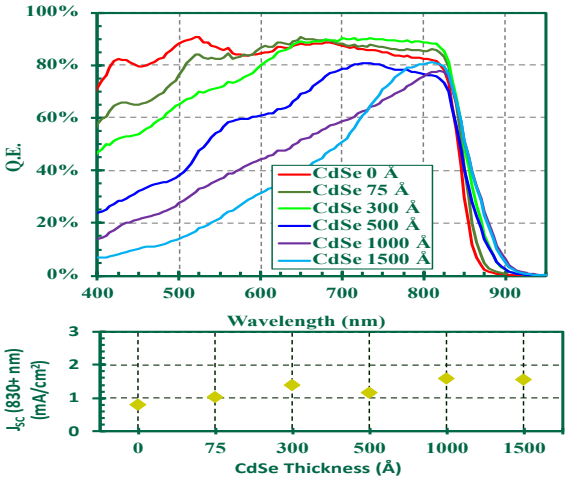


Figure 44 The SR data shows CdSe thicknesses from 0 to 1500 Å form CST by inter-diffusion.

6.2 The Study of CdSe/CdTe Bi-Layer on the Devices Performance

In CdS/CdTe solar cells, the $CdCl_2$ HT promotes inter-diffusion at the CdS/CdTe junction, which improves the electronic properties of the junction by reducing the lattice mismatch, stress, and interface recombination [113]. In this work, the effect of $CdCl_2$ HT has been investigated for four different annealing temperatures (390, 410, 430, and 450 °C). The thickness of CdSe is another critical parameter that influences the properties (composition) of the $CdSe_xTe_{1-x}$ layer formed as a result of inter-diffusion between CdTe and CdSe. It can determine the Se distribution in $CdTe_{1-x}Se_x$ and the resulting bandgap of the absorber at the junction interface. To date, the CdSe thickness has been varied from 75 to 1500Å. Figure 45 shows the JV and SR for $CdSe_xTe_{1-x}$ devices fabricated with different CdSe thicknesses and $CdCl_2$ HT at the temperature of 410°C. Both the V_{OC} and FF decrease with increasing CdSe thickness. The redshift in SR for devices with higher CdSe layer thicknesses indicates a reduction in the bandgap of the absorber as expected in

$CdSe_xTe_{1-x}$ alloy due to bowing effect. However, the devices with thicker CdSe (> 300 Å) show lower carrier collection in the blue region. This is believed to be due to residual CdSe not fully consumed via inter-diffusion with CdTe (i.e. CdSe/CST/CdTe), which might also explain the lower V_{OC} and FF of the devices. The drop in V_{OC} for thicker CdSe is also reported by other groups [114]. Similar results are observed for devices $CdCl_2$ HT at 390 °C. Figure 46 (left) shows the SR of devices with $CdCl_2$ HT at 430 °C. These results suggest that CdSe is fully inter-diffused for all thicknesses, as indicated by the increased carrier collection in the blue region. The QE at long wavelengths increases with increasing CdSe thickness. This clearly demonstrates that the bandgap decreases gradually with increasing CdSe thickness indicating an increase in the composition (x) of $CdSe_xTe_{1-x}$. This redshift is greater compared to devices annealed at lower temperatures for the same CdSe thicknesses (see Figure 45). The corresponding bandgaps calculated from the absorption edge for all the devices with different CdSe thicknesses and $CdCl_2$ heat treatment temperatures are shown in Figure 46 (right). For 390 and 410 °C HT, there is a slight decrease in bandgap with increasing CdSe thickness, which appears to level off at larger thicknesses. The largest bandgap reduction occurs at a temperature of 430 °C. The smallest bandgap (1.36 eV) corresponds to the device with the thickest CdSe of 1500 Å. Additional increases in the $CdCl_2$ HT temperature (450 °C) to further reduce the bandgap resulted in flaking and delamination for the majority of the films.

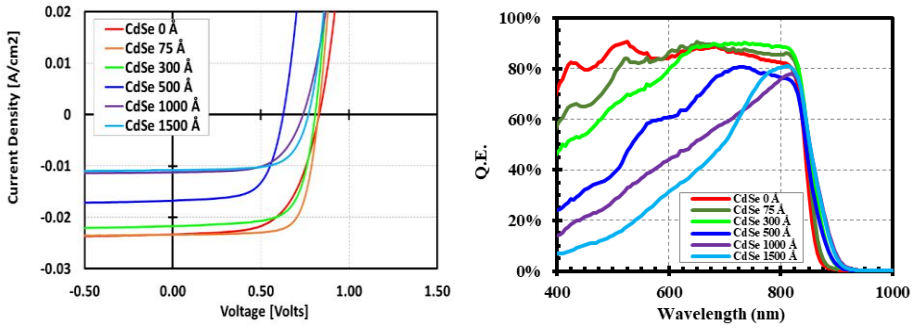


Figure 45 The (left) JV and (right) SR measurements in the various CdSe thicknesses (0Å to 1500Å) on CST/CdTe devices.

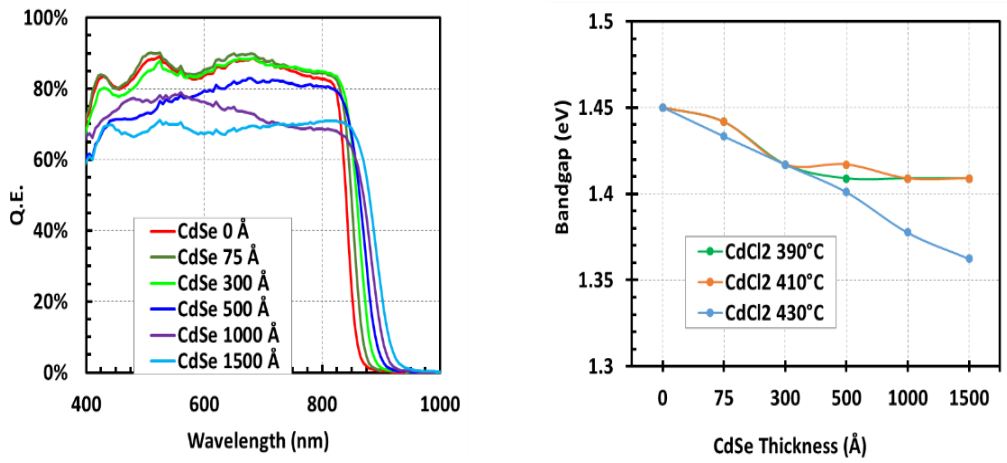


Figure 46 The (left) SR and (right) bandgap data for $CdSe_xTe_{1-x}$ devices with different deposited CdSe thicknesses (0/75/300/500/1000/1500Å) in the $CdCl_2$ heated treatment temperature at 430°C.

A summary of the cell results is shown in Table 6.1.

Table 6.1 Device performance for various CdSe thicknesses.

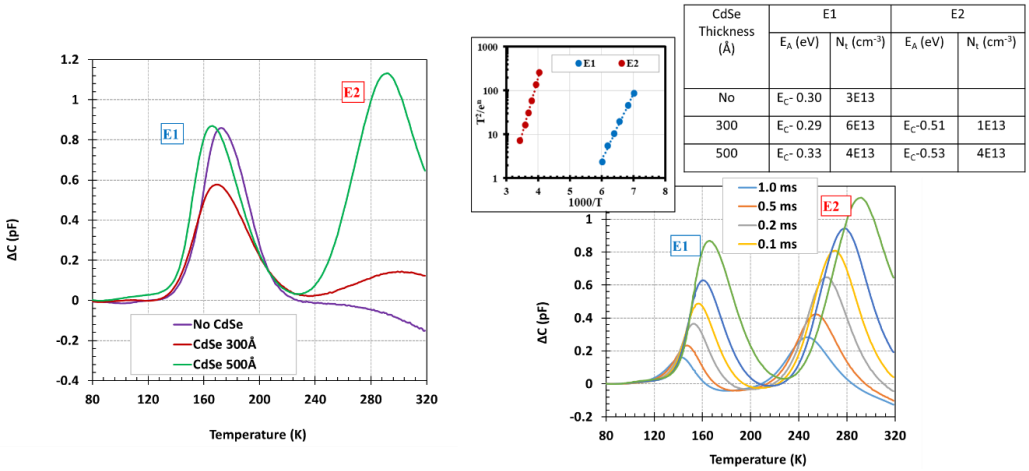
CdCl2 HT (°C)	CdSe Thickness (Å)	V_{OC} (mV)	FF (%)	J_{SC} (mA/cm^2)	η (%)
390	0	830	67.2	23.78	13.22
	75	810	69.1	24.43	13.65
	300	740	66.4	23.33	11.39
	500	620	58.2	19.20	6.90
	1500	650	57.0	14.49	5.37
410	0	830	61.3	24.77	12.54
	75	830	74.1	24.28	14.91
	300	810	69.0	23.39	13.07
	500	630	64.0	18.32	7.39
	1500	770	68.3	12.77	6.68
430	0	770	54.2	24.55	10.21
	75	800	55.7	25.43	11.19
	300	840	54.2	25.49	11.56
	500	790	44.3	23.91	8.31
	1500	690	40.0	21.98	6.07
450	0	730	23.2	23.54	3.95
	75	740	24.6	25.81	4.58
	300	780	26.2	25.80	5.23
	500	Film damage			
	1500	Film damage			

6.3 Defect Analysis of CdSe/CdTe Devices

DLTS measurements have been performed on selected samples to analyze the deep defect distribution. The devices are chosen based on the following two criteria – normal JV behavior (no 'kink,' roll-over, etc.) and fully inter-diffused CdTe/CdSe bilayer, as indicated by the SR data. Figure 47 (left) shows the DLTS spectra for devices $CdCl_2$ heat treated at 410 °C with different CdSe thicknesses. The spectra for the device without CdSe is identical to baseline CdS/CdTe devices. The positive peak in the temperature range 150-200K indicates a minority carrier trap (E1). This shallow trap (E_A ~ 0.3eV) has been attributed to Cl_{Te} [115]. The negative ΔC near room temperature indicates a deep majority carrier trap. For devices with CdSe, an additional positive peak is observed at temperatures above 240K. This indicates a deeper minority carrier trap (E2). The DLTS measurements are performed at six different rate windows to calculate the activation energy. Figure 47 (right) shows the different rate window spectra for the device with 500 Å CdSe. The trap activation energy is calculated from the Arrhenius plot of the peak positions at different rate windows (Figure 47 insets). The increasing intensity of E2 with CdSe thickness suggests the formation of a Se related complex defect. This deep minority carrier trap (E_A ~0.52 eV) may have a compensating effect; however, since it is known that minority carrier lifetimes in $CdSe_xTe_{1-x}$ are higher compared to CdTe films, this Se related defects are not expected to impact lifetimes referred to later TRPL measurements [116]. Figure 47 (table) lists the calculated activation energies and traps concentrations for these defect Capacitance-Voltage (CV) measurements for the devices (Figure 48) shows the effect of CdSe thickness on the doping concentration. There is an initial (small) increase in carrier concentration for CdSe thickness up to 300 Å. Higher CdSe thicknesses result in reduced doping; this reduced doping may be due to the E2 defect discussed above. The same trend was observed for all $CdCl_2$ HT temperatures. This is possibly due to an increase in the

concertation of the deep minority carrier trap observed in the DLTS measurement (Figure 47) for thicker CdSe devices. Preliminary results from minority carrier lifetime measurements are shown in Table 6.2. Comparison between the two samples heat treated at 410 °C with and without CdSe indicate that CdSe improves the minority carrier lifetime. Similarly, for the 75 Å CdSe devices, increasing the $CdCl_2$ HT temperature to 410 °C shows improved lifetime. This suggests that both $CdCl_2$ HT temperature of 410 °C and a low Se content $CdSe_xTe_{1-x}$ alloy improves lifetime. Therefore, at the low thickness of CdSe net p-type doping concentration (CV) and minority carrier lifetime (TRPL) increase. Such devices show better V_{OC}'s; however, no significant current gain is observed due to the small amount of CdSe that did not result in significant bandgap reduction. Increasing the CdSe thickness results in lower p-type doping. Thicker CdSe results in higher J_{SC}, but exhibits lower V_{OC} and FF, possibly due to a combined effect of low doping, deep defects, and the smaller bandgap of the $CdSe_xTe_{1-x}$ alloy. Therefore, an optimum CdSe thickness ($CdSe_xTe_{1-x}$ alloy) must be achieved that can maximize J_{SC} without losses in V_{OC}. The best $CdSe_xTe_{1-x}$ based cell fabricated to-date exhibited V_{OC}= 850 mV, J_{SC}= 26.3 mA/cm^2, FF= 73 % and efficiency 16.3%.

The effect of $CdCl_2$ HT and CdSe thickness on the performance of $CdSe_xTe_{1-x}$ photovoltaic devices has been investigated. Devices with small amount of CdSe shows higher doping and minority carrier lifetime, however with no significant current gain. Both higher $CdCl_2$ annealing temperature and larger CdSe thickness appear to promote CdSe-CdTe inter-diffusion and improve collection in the red region due to the reduction of absorber bandgap. Lower V_{OC} in thick CdSe devices has been attributed to the reduced bandgap, low doping, and the presence of deep defects. An optimized CdSe thickness and $CdCl_2$ HT temperature can lead to both improvement in V_{OC} and J_{SC} and thus improved efficiency.



CdSe Thickness (Å)	E1		E2	
	E_A (eV)	N_t (cm^{-3})	E_A (eV)	N_t (cm^{-3})
No	E_C- 0.30	3E13		
300	E_C- 0.29	6E13	E_C-0.51	1E13
500	E_C- 0.33	4E13	E_C-0.53	4E13

Figure 47 The (left) comparative DLTS spectra for devices $CdCl_2$ treated at 410 °C with and without CdSe, obtained with a rate window of 0.02 ms. The (right) DLTS spectra for CdTe device with 500 Å CdSe at 6 different rate window. The corresponding Arrhenius plot to calculate the defect activation energy is shown on the inset.

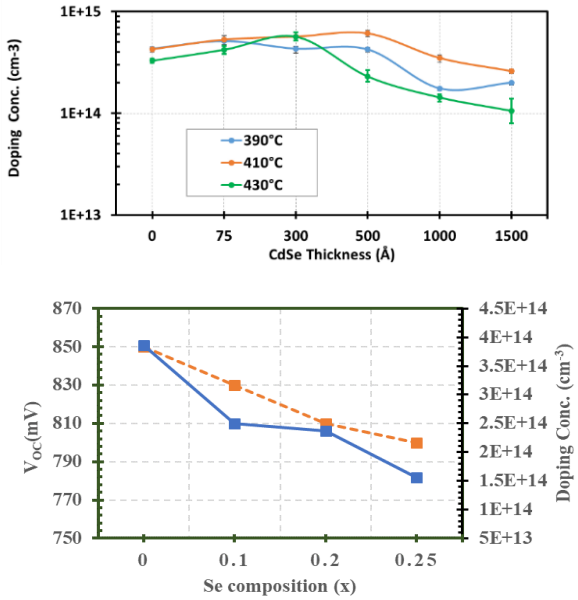


Figure 48 P-type net doping concentration for devices with various $CdCl_2$ treatment temperatures (390 to 430 °C) and Se compositions.

Table 6.2 Minority carrier lifetime for different CdSe/CdTe devices.

$CdCl_2$ HT (°C)	CdSe Thickness (Å)	Minority Carrier Lifetime (ns)
390	75	10
410	0	11.1
410	75	13.8

6.4 Se Profile Study of CdSe/CdTe Devices

Se profiles in CST ($CdSe_xTe_{1-x}$) films which is fabricated by annealing CdSe/CdTe bi-layers has been investigated using transmission electron microscopy (TEM) and energy-dispersive X-Ray spectroscopy (EDS). The thickness effect of CdSe layer was studied on the CST alloys with the relationship of $CdCl_2$ annealing conditions. The CdSe thickness was varied from 75 to 1,500 Å. Compared with the "thin" films (CdSe 75-300 Å), all "thick" films (CdSe>300 Å) revealed decreased grain structure at the interface junction. However, the "thin" films exhibited larger columnar grains which similar with regular CdTe structure that extended through the CST/CdTe interface. The alloy layer for "thick" CdSe films appeared as a bilayer with two CST compositions: Se-rich and Te-rich region, respectively. As mention above, the CdSe/CdTe devices revealed Se related defects in the films with thicker CdSe (1,000 and 1,500 Å). The Se compositional profile was found to be greatly dependent on the CdSe thickness and $CdCl_2$ heat treatment conditions. Due to the formation of voids at the interface with large CdSe thicknesses (> 300 Å), it is believed Se composition of CST alloys must be kept *low* to avoid performance degradation.

Cross-section TEM characterized the devices for the study of grain-structure and elemental distribution with various CdSe thicknesses. Figure 49 exhibits the EDS analysis on the Se composition at the different regions across CdSe/CdTe bi-layer with varying CdSe thicknesses: 150, 300, 1000, and 1500 Å. The $CdCl_2$ HT was conducted at 410 °C for the thin CdSe films (<150 Å) and the temperature increased to 430 °C for all thicker films (>300 Å) (lower $CdCl_2$ anneal temperatures for thick CdSe films resulted in incomplete interdiffusion; i.e., not all CdSe was consumed). The Se composition increases with the thickness of the CdSe layer, as seen from left to right in Figure 49. In addition, Se diffuses deeper into the CST film, as anticipated because of more aggressive $CdCl_2$ annealing treatment. If the CdSe films are thicker (1,000 and 1,500 Å),

the Se composition became inhomogeneous. Each region of Se-rich and Te-rich was identified by the location of proximity to CdSe or CdTe side. For example, in the CdSe side within 0.5 μm, the Se composition is higher than the CdTe side of the metallurgical junction for the CST alloys. The EDS mapping of CdSe (1,500 Å)/CdTe devices with the highest $CdCl_2$ HT at 430 °C is shown in Figure 50. The results also show that Cl diffused throughout the CdSe/CdTe absorber and appears to accumulate at the CdS/CST interface and the grain boundaries. The MZO layer retained intact, indicative of no elemental diffusion throughout the material. The same E-image exhibits in the profiles of Se and S, which proceeds inter-diffusion in the film stack, respectively. Thus, for the Se-rich region of the CST alloy, it is believed to contain both S and Se elements after the inter-diffusion process. The Te concentration was found (from EDS line-scanning analysis not presented here) to decrease in this region.

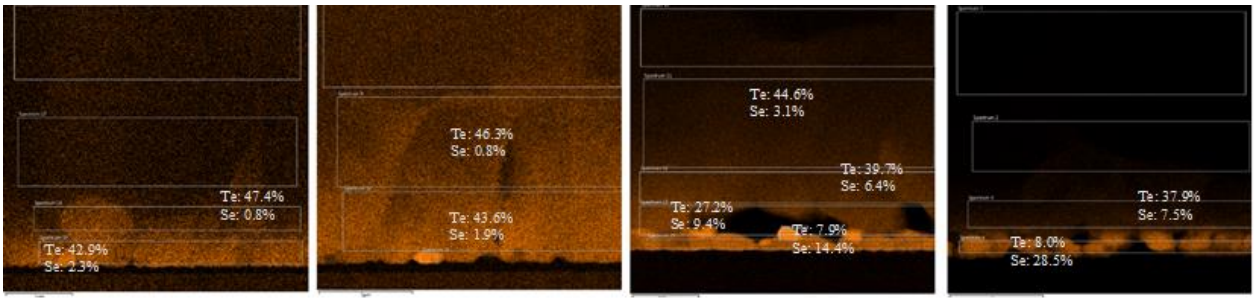


Figure 49 Compositional maps for CST films produced with CdSe films of various thicknesses (150, 300, 1000, and 1500 Å from left to right).

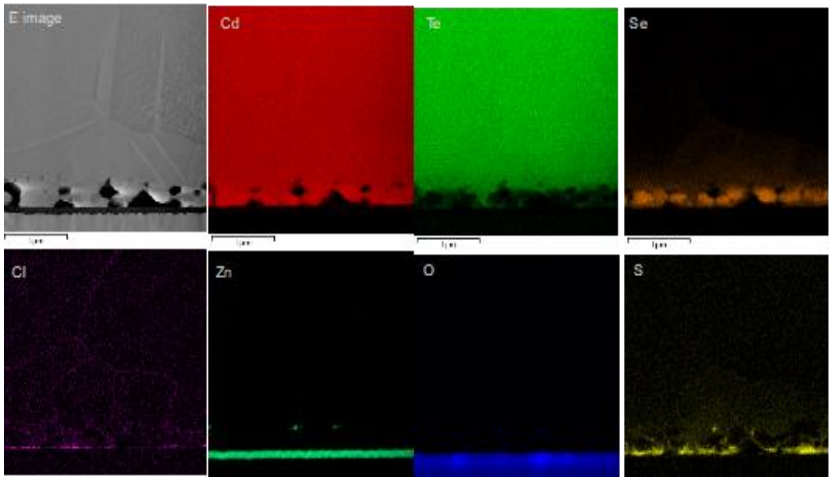


Figure 50 EDS elemental mapping for a CST film produced with CdSe thickness (1500 Å).

Figure 51 shows that the CST and CdTe grains are larger when the CdSe layer was "thin" (150 and 300 Å). The grains also extended throughout the entire CST/CdTe stack. No particular stacking faults were present in the CST/CdTe absorber layer after the inter-diffusion process, regardless if twin grains were present. In comparison, as the CdSe thickness increased (1,000 and 1,500 Å), the large columnar grains no longer extended throughout the entire absorber layer structure at the CST/CdTe junction. A region of small grains was observed above the junction interface which is the CST alloy. The coverage of the CST/CdTe region appeared to be non-uniformed across the MZO layer, and the presence of voids is evident at the interface.

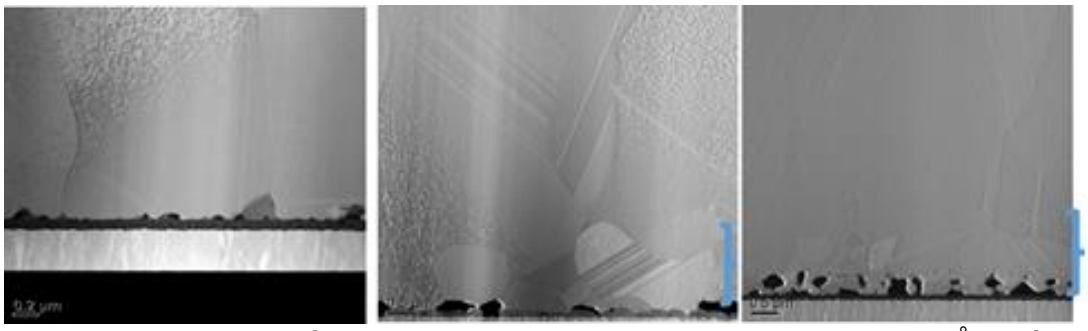


Figure 51 STEM images for three CdSe thicknesses (300, 1,000, and 1,500 Å) (left to right) showing variations in the grain structure.

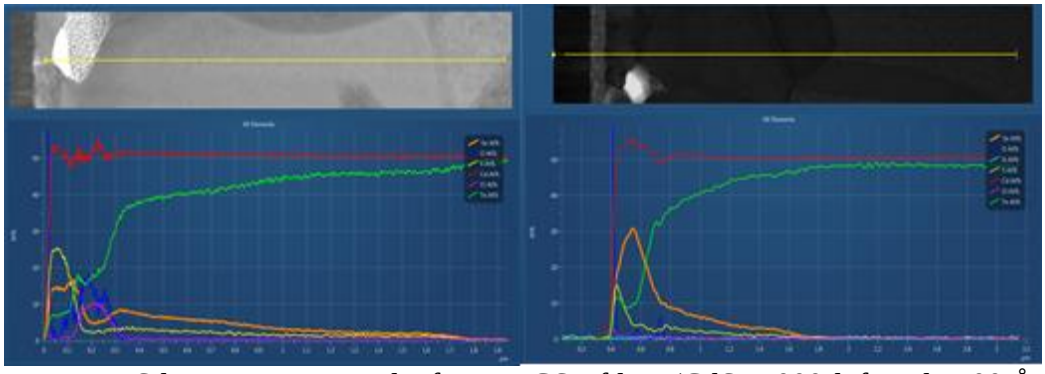


Figure 52 EDS line scanning results for two CST films (CdSe 1000-left and 1500 Å- right) produced in a $CdCl_2$ HT temperature at 430 °C.

The EDS line scans are presented in Figure 52 for two samples with different CdSe thicknesses (1,000 and 1,500 Å). The concentration of Se increased for the structure with the thicker CdSe film. The entire inter-diffusion can be confirmed in the EDS line scan profile, which

revealed the Se concentration gradually decreased within the first micrometer of the CdTe layer to form the CST alloy. The variation in the Se diffusion profiles emphasizes the effect of the CdSe thickness in forming a homogeneous CST alloy, especially at higher $CdCl_2$ annealing temperatures. In addition, the inter-diffusion process is extensive at higher $CdCl_2$ HT temperatures (> 420 °C); however, the devices showed the degradation of the junction quality via the formation of voids. The formation of the voids at the CdSe/CdTe interface is due to a mechanism called *"Kirkendall effect,"* which is the result of inter-diffusion between two semiconductor materials that have entirely different diffusion rates of the atoms [117]. The poor quality of the CdSe/CdTe interface structure was taken in the cross-section images for the thick CdSe (>300 Å) layer, show several voids in the CST region. Devices with "thick" CdSe (> 300 Å) had been previously found to have poor open-circuit voltage (V_{OC}), likely attributed to the inhomogeneity of the CST alloy and the voids (in addition to the decreased bandgap).

The device performance was exhibited in Table 6.5 shows that J_{SC} can improve to above 28 mA/cm^2 at lower $CdCl_2$ HT temperatures (< 430 ℃). The device J_{SC} increased at high Se compositions (approx. 15%), due to a reduction in the CST bandgap; recent samples were deposited the CST alloys by direct sublimation with Se composition of 40% (to be discussed later) have reached J_{SC} approximately 30 mA/cm^2, clearly indicating the composition effect of CST in improving the cell current due to carrier collection in the long wavelengths. Figure 53. exhibites the Spectral Response (SR) and Light Current-Voltage (J-V) measurements for cells. The devices were fabricated with CST alloys which are synthesized with CdSe thickness (1000 Å) and annealed at three various $CdCl_2$ temperatures. The CdSe is believed to have been completely consumed via inter-diffusion for all $CdCl_2$ annealing temperatures as evidenced by the red shift in SR @ 880 nm shown in Figure 53 (right). The appearance of a *"kink"* in the JV data suggests that the presence

of a barrier (a discontinuity on the conduction band) for the cell annealed at the highest temperature; thus in order to improve the device performance, the CST composition/formation and the buffer/window layer have to be simultaneously optimized.

Table 6.3 Device performance for various $CdCl_2$ HT.

CdSe Thickness (Å)	Voc (mV)	FF (%)	Jsc (mA/cm^2)	Efficiency
$CdCl_2$ HT 390°C	790	54.70%	27.25	11.78
$CdCl_2$ HT 410°C	790	63.80%	28.03	14.13
$CdCl_2$ HT 430°C	800	34.40%	26.02	7.16

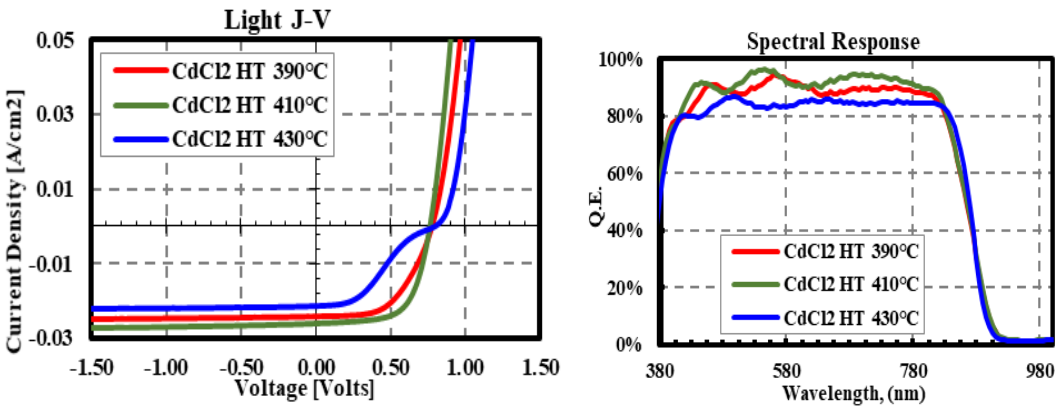


Figure 53 Light J-V and SR for three devices fabricated with 1000 Å thick CdSe and annealed at different $CdCl_2$ temperatures (390 to 430 °C).

The effect of CdSe thickness on the Se profile in CST alloys, which are formed by various $CdCl_2$ HT for CdTe/CdSe bi-layers has been studied. TEM and EDS analysis both supported that CST films synthesized with "thin" (< 300 Å) CdSe films resulted in well inter-diffused CST films and a homogeneous grain structure which contributed to the uniform CST alloy. Thick (> 300 Å) CdSe films resulted in CST alloys with random smaller grain at the interface and inhomogeneous Se profiles, with a Se-rich region and Te-rich region. Also, the thick CdSe (> 300 Å) lead to the presence of voids at the interface, which is detrimental to device performance. These poor interface

junction can be used to point out the loss in V_{OC} for devices fabricated with CST films synthesized via annealing of CdTe/CdSe bilayers. In the next chapter, the direct sublimation of CST alloys is described as an improved approach for the formation of MZO/CST/CdTe junctions.

CHAPTER 7

$CDSE_XTE_{1-X}$ BY DIRECT SUBMILATION OF CST ALLOY

The alloying of CdTe with CdSe for the formation of CST has been found to improve carrier lifetimes, which is a requirement for obtaining high V_{OC}. The smaller bandgap of CST (E_g= 1.36 - 1.41 eV) results in higher J_{SC}, but is also expected to lower the limit of the maximum attainable V_{OC}. It was also found that net p-type doping in CST is lower when compared to similarly processed CdTe devices, which can also lower V_{OC}. Grading of CST alloys can be used to enhance carrier collection, which is an additional benefit from the use of CST alloys [118]. The bulk of absorber has gradually increased in conduction bandgap can be associated with grading CST alloys of various Se composition and CdTe from the front of the junction by achieving the best performance. One of the requirements to achieve high efficiency $CdSe_xTe_{1-x}$/CdTe solar cells is the quality (homogeneity, point defects, etc.) of the alloys and the doping concentration [119]. It was described in the previous chapter that CST films fabricated using inter-diffusion of CdTe with CdSe layers resulted in the formation of voids at the *"junction,"* inhomogeneous composition, and *"unused"* CdSe (incomplete interdiffusion). The quality of CST can be improved via direct deposition (i.e. not interdiffusion of bi-layers) using the Close Spaced Sublimation (CSS) deposition and CST alloys as the source materials [120]. This can result in homogenous CST alloys, and improved control of the junction interface (MZO/CST). The CSS process offers a means of controlling the grain size, therefore enabling improved lifetimes due to the reduction in grain boundaries [121]. Despite the various competing mechanisms discussed above – i.e. smaller bandgap that can lead to higher J_{SC} but lower V_{OC}, decrease in net doping with Se concertation etc.

- the CSS offers the flexibility to optimize the properties of CST for maximum performance (grain size/structure, lifetime etc.).

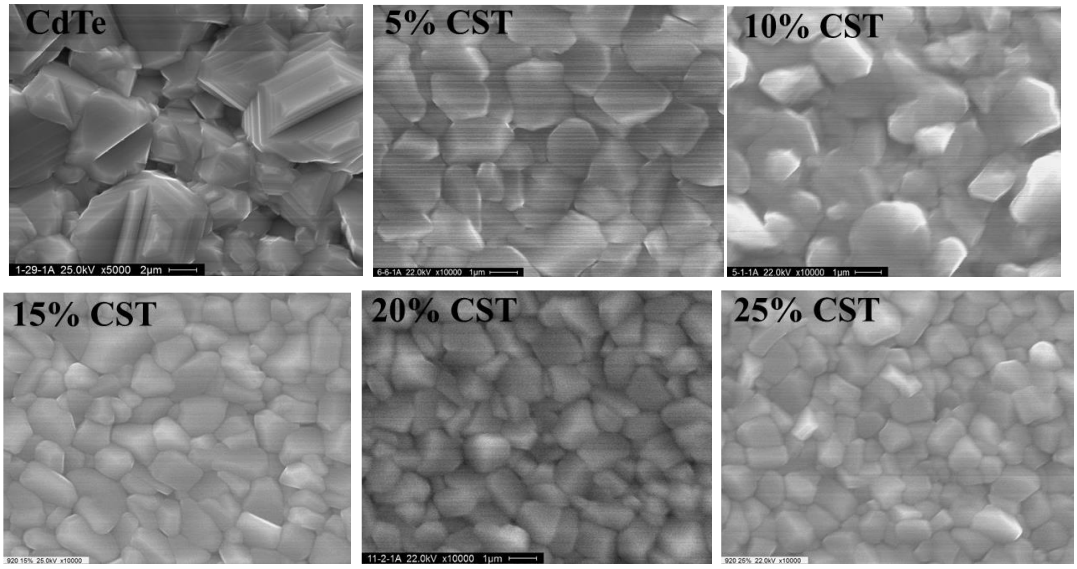


Figure 54 SEM images show the CST alloy with 5 to 25% of Se incorporated CdTe respectively.

7.1 Effect of CST Composition (x)

The surface morphology/grain structure of CST films (approx. 3 µm) with various Se compositions are shown in Figure 54. It can be seen that increasing the Se composition ($0 \leqq x \leqq 25$ %) of the $CdSe_xTe_{1-x}$ alloys results in a decrease in the grain size. Therefore, the structural and morphological properties exhibit a strong dependence on the alloy composition (x) [120]. Figure 55 shows that increasing the Se composition (x) results in a gradual shift of the (1 1 1) peak from CdTe side to CdSe, as expected. Using the XRD data, the lattice constants for the various alloys were calculated (Å) and are shown in Figure 56 (Lattice constants for CdTe (6.48 Å) and CdSe (6.08 Å)) The XRD peaks (1 1 1) also exhibited broadening with increased Se composition (x) suggesting a decrease in the grain size. The grain size of CST films was calculated using equation (19) below and compared to SEM analysis. The calculated grain sizes for the various Se compositions are shown in Table 7.1, which have been validated by both XRD and SEM data.

$$\text{Size} = \frac{K\lambda}{Width * \cos\theta} \qquad (19)$$

Using the lattice constant calculated from the XRD data above, the composition of CST alloys was also obtained using Vegard's Law (equation 20 below):

$$a(x) = xa_{CdSe} + (1\text{-}x)a_{CdTe} \qquad (20)$$

where a(x), a_{CdSe} and a_{CdTe} are the lattice constants of the $CdSe_xTe_{1-x}$, CdSe and CdTe, respectively. The corresponding compositions were shown in the analytical data which are within 5% of the values obtained using EDS analysis exhibit in Table 7.2.

Table 7.1 The grain size with various Se composition (x= 0 to 25%) of $CdSe_xTe_{1-x}$ films.

x (%)	Grain Size (XRD) (µm)	Grain Size (SEM) (µm)
0	6.10	6.00
5	3.21	3.00
10	2.54	2.50
15	2.06	2.00
20	1.45	1.50
25	1.24	1.30

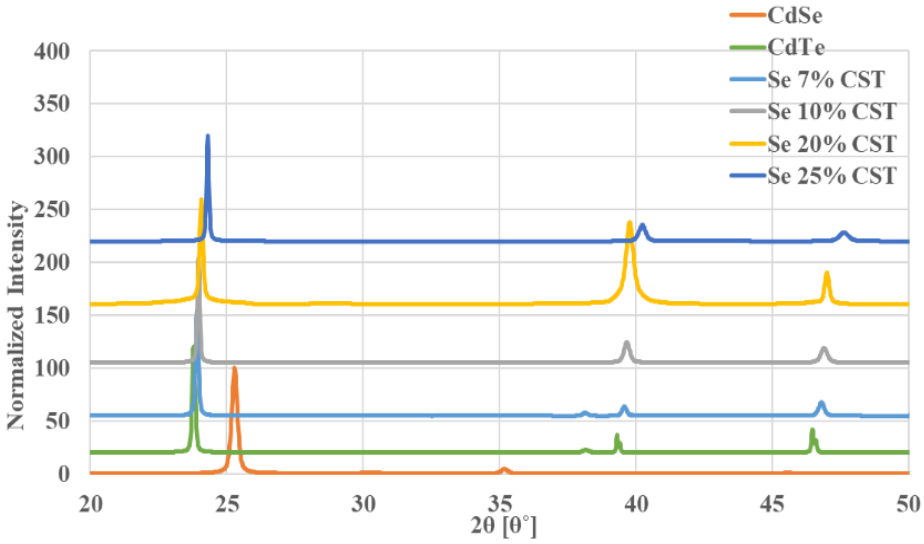


Figure 55 XRD patterns of CST films [0 ≦ x ≦ 1] grown on glass substrates.

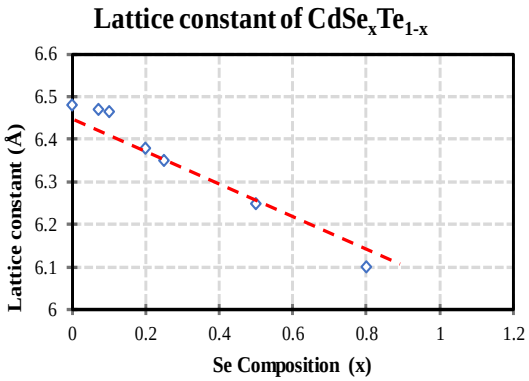


Figure 56 The lattice constant of CST films [0 ≦ x ≦ 1] grown on glass substrates from XRD preferred peak (1 1 1).

Table 7.2 The Vegard's Law vs. EDS analysis for various Se compositions.

x (EDS) (%)	2θ (deg)	$a_{d\ (111)}$ (Å)	x (XRD) (%)
6.45	24.05	6.47	6.95
10.52	24.11	6.46	11.01
19.65	24.27	6.38	20.52
25.12	24.43	6.35	25.41

It is well known that the addition of S or Se into CdTe to form the ternary compounds it initially results in lower optical bandgap due to the bowing effect. The energy gap of the CST allows us shown in Figure 57; the red dotted line represents theoretical calculation from, and the blue diamonds are data points measured from this work.

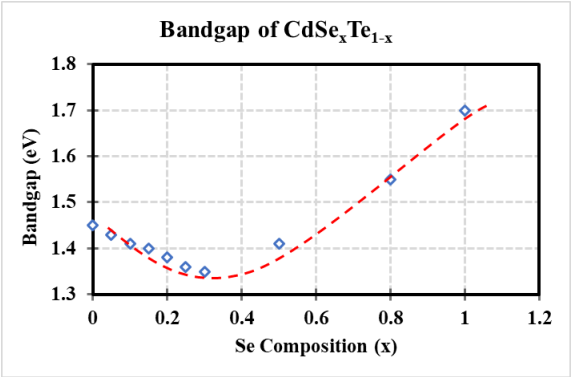


Figure 57 Optical bandgap of $CdSe_xTe_{1-x}$ films [0 ≦ x ≦ 1] deposited on glass substrates by CSS technique.

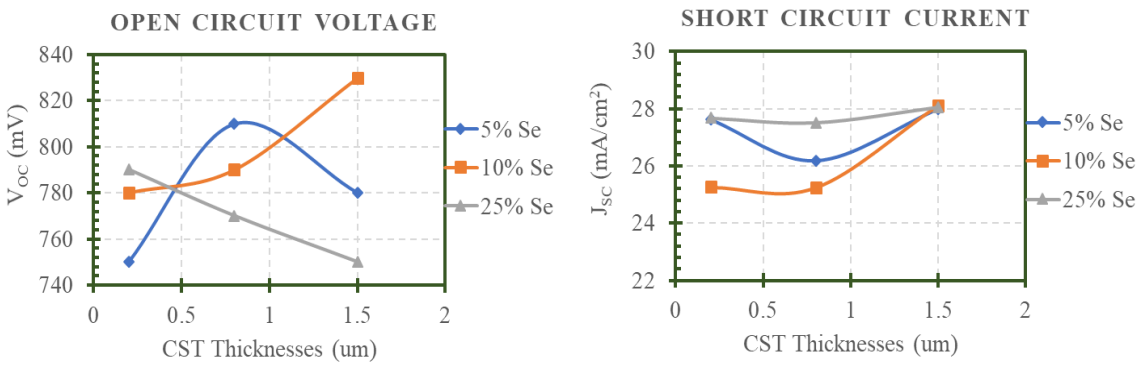


Figure 58 The (left) open-circuit voltage and (right) short-circuit current data in different CST alloys thicknesses (0.2 to 1.5 um).

7.2 The Thickness Effect on CST Devices (Direct CSS)

The effect of the CST thickness on device performance is summarized in Figure 58 for three Se compositions (5, 10, and 25%). The V_{OC} is all exhibited relatively low in the thicknesses of CST layer (< 1.0 um) for all Se compositions. However, the CST thickness is increased, and it is believed to be beneficial to improve the V_{OC}. In the J_{SC}, as increasing CST thickness, the current is slightly increased for all Se compositions due to the more carrier collection in the long wavelength that is shown in Figure 59. The effect of CST thickness will be further investigated.

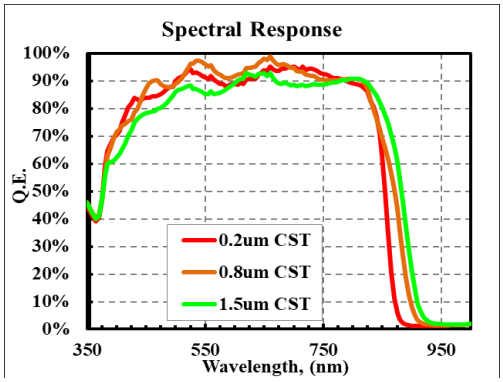


Figure 59 Spectral response for various CST thicknesses in the 10% Se compositions.

7.3 Effect of CSS Ambient and Substrate Temperatures on CST

The quality of CdTe and CST films using CSS depends on the ambient pressure and substrate temperatures, both of which influence the grain structure of the thin films. Since the grain size decreased with the addition of Se, the possibility to increase the grain size via the ambient gas

and substrate temperature have been investigated. Figure 60 shows the SEM micrographs of CSS CST films prepared at four substrate temperatures (550, 600, 620, and 640 ℃). The film deposited at 620 ℃ consists of relatively large grains 3-4 µm in size and is dense. The film deposited at 500 ℃ consists of much smaller grains which appear to coalesce in clusters of approximately 1 µm in size. Overall, the grain size increased as the T_{SUB} increased from 550 to 620 ºC. The largest grains were observed for the 620 ºC in Se composition (x= 25 %). Therefore, it is possible to utilize the CSS substrate as a means for controlling the grain size.

The addition of O_2 as ambient gas during the CSS deposition, shifts CSS from diffusion-limited to reaction-limited growth, primarily through source oxidation. The main benefits of oxygen in CdTe films has been found to be passivation of donors and defects, increase in acceptor density, and reduction in the grain size. The incorporation of O_2 also lowers the sublimation rate and has been found to increase in the number of nucleation sites, and it can, therefore, be utilized to control the film grain size.

The X-ray diffraction patterns of as-deposited CST alloys (x= 25%) films are shown in Figure 61. The films were deposited in He/O_2 ambient at a T_{SUB} between 550 to 640 ºC. The CST samples have a cubic zinc-blende structure due to the Se composition being below 60 %. The as-deposited CST films exhibited a strong preferred orientation along the (1 1 1) planes parallel to the substrate. For the samples deposited at T_{SUB} 620 ºC, the peak (1 1 1) had a narrow FWHM which indicates larger grain size with increasing T_{SUB}. The change in T_{SUB} did not cause a shift in the (1 1 1) peak; therefore the lattice constant and composition were found to be independent of T_{SUB} (within the range of temperatures studied to-date). The preferential orientation of the CST along the (1 1 1) direction improved at higher T_{SUB} as indicated by the higher relative intensity of this peak.

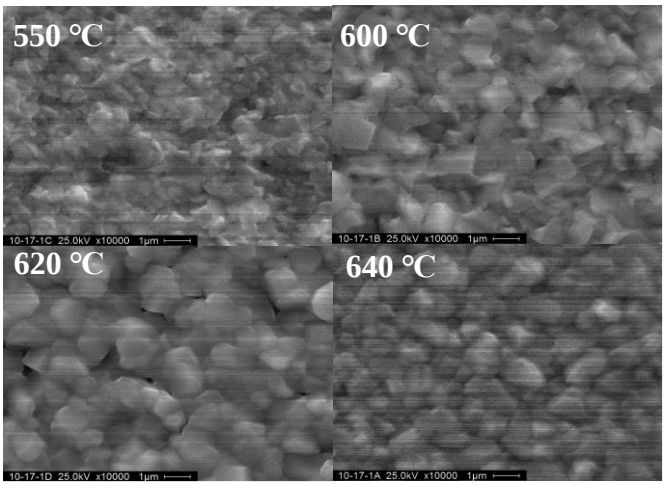


Figure 60 The SEM images of CST alloys in various substrate temperatures at He/O_2 ambient gas.

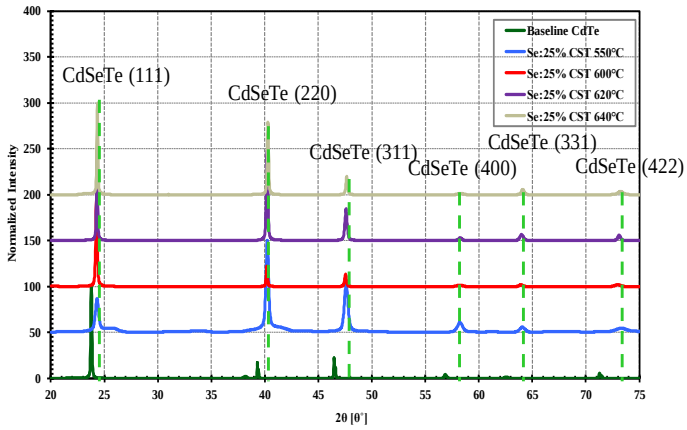


Figure 61 The XRD pattern of CST (25% Se) deposited on MZO/ITO glass substrates in various T_{SUB} at He/O_2 ambient gas.

Table 7.3 The performance of devices for various substrate temperatures (CST x=25%).

T_{SUB}	V_{OC} (mV)	FF (%)	J_{SC} (mA/cm^2)	Efficiency (%)	Bandgap (eV)
550°C	800	56.20	28.57	12.85	1.37
600°C	810	58.50	28.61	13.56	1.37
620°C	830	64.50	29.21	15.64	1.38
640°C	810	54.80	28.64	12.71	1.39

7.4 CST/CdTe Bilayers

CST/CdTe bilayers, similar to structures used for solar cell fabrication, were also prepared. CST alloys deposited at T_{SUB} from 550 to 640 ºC, followed by a CdTe deposition at T_{SUB} (580 ºC) and T_{SOU} (680 ºC) by CSS respectively. Figure 62 shows cross-sectional STEM images for these structures. Firstly, the grain size for the CST films adjacent to the junction becomes more significant with increasing temperatures. For the higher temperatures, the grain structure is similar to CdTe with large grains extending through the thickness of the entire bi-layer CST (x=25 %)/CdTe, and there is no clear boundary between CST and CdTe. However, at the lower temperature, the CST alloy consists of smaller grains than CdTe, and there is a clear boundary between CST and CdTe. In contrast to these CST/CdTe bilayers, CST films formed by post-deposition interdiffusion of CdSe/CdTe layers exhibited significant void formation due to the *"Kirkendall effect"* [117]. As it will be discussed in the next section, solar cell performance improved for devices fabricated with CST deposited at high temperatures.

Figure 63 shows EDS line scans for CST films deposited at T_{SUB} 620 ºC with Se composition (x=25 %) (thicknesses 2± 10% µm) as well. The two films were annealed at different $CdCl_2$ temperatures (410 and 430 ºC). The Se profile for the film annealed at 410 ºC exhibits a sharp drop at approx. 1.8 um suggesting that Se out-diffusion from CST to CdTe is limited, while the film annealed at 430 ºC clearly shows a gradual decrease in the Se profile concertation that is suggesting that the $CdCl_2$ annealing temperature can be used for grading the Se composition. In conclusion, for the low $CdCl_2$ HT temperature, the entire inter-diffusion could be confirmed in the EDS line scan profile, which revealed the Se concentration do not decrease within the first micrometer of the absorber layer for the bulk of CST alloy. On the other hand, in order to effectively passivate the grain boundaries and engineer the grading CST layer, the CST alloy is

required to fabricate at aggressive $CdCl_2$ HT temperatures (430 °C). Therefore, it is feasible to achieve uniform films without degrading the junction quality via the formation of voids by implementing inter-diffusion of bi-layer CdSe/CdTe [119].

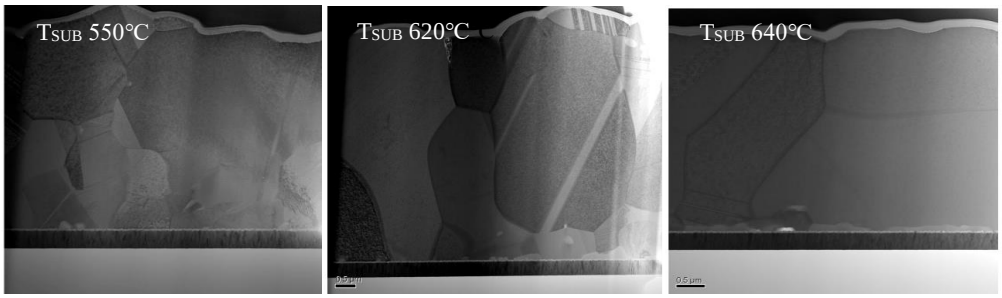


Figure 62 The STEM images of CST alloys in various T_{SUB} (550 - 640 ºC) at He/O_2 ambient showing variations in the grain structures.

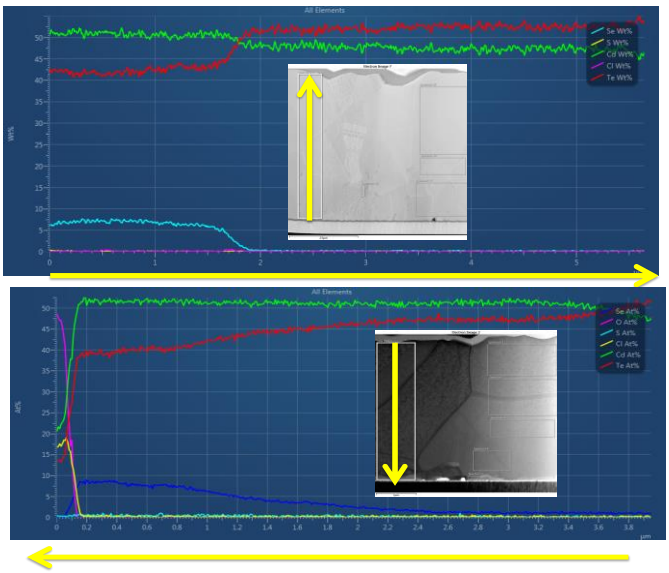


Figure 63 The EDS line scanning of CST (25% Se)/CdTe devices at T_{SUB} (620 ºC) in $CdCl_2$ HT at 410 (up) and 430 °C (down) respectively.

7.5 The Study of CST on the Devices Performance

Device performance for several cells fabricated with CST/CdTe bi-layers (x=25%) is presented in Table 7.3. J_{SC} was calculated from integrating the QE data using AM1.5. The last column shows the amount of J_{SC} generated by absorption beyond the CdTe bandgap (i.e., @ wavelengths >855 nm). In all devices, the increase due to the bandgap change in CST was > 4.0

mA/cm^2. The spectral response (SR) for the cells listed in Table 7.3 is shown in Figure 64 (right). The shift in the SR data at the absorption edge is small ($\Delta\lambda$=13 nm), corresponding to a bandgap change of <0.02 eV as shown in Table 6.2. However, the absorption edge (optical bandgap) slightly changes from 1.37 to 1.39 eV, which indicated the effect of fabrication process alternate the Se diffusion profile of CST alloy after completing the cells. From the EDS analysis and XRD lattice constants calculation showed the Se compositions were no apparently changed before completing cells in various T_{SUB} for CST alloys depositions. Increasing the Se composition to 40% leads to J_{SC} > 30 mA/cm^2 (cells not shown here), clearly demonstrating the role of CST in increasing the cell current; however, the V_{OC} decreased to 770 mV. The effect of substrate temperature on the V_{OC} is seen in Table 7.2 and Figure 64 (left) that shows the light J-V for the same cells. The V_{OC} initially improves with increasing T_{SUB} and decreases for the highest temperature of 640 ℃. The initial increase can be explained partly on (a) the improved grain structure near the interface (as the temperature increases) as shown in the previous section, and (b) to a lesser extent due to the small bandgap increase shown in Table 7.2. Another reason is p-type net doping dependent, which was exhibited where the V_{OC} and net p-type doping as a function of substrate temperatures are shown in Figure 65 (left). The data suggests that the substrate temperatures for CST deposition, it is believed to affect the p-type net doping on the devices, with an optimum substrate temperature of 620 ℃ for x=25 % CST alloy obtained at V_{OC} of 830 mV and p-type net doping approximate 2.90E+14 cm^{-3}. However, the devices of net p-type doping are not a significant influence in various T_{SUB} for increasing the V_{OC} in this experiment due to a small change of doping concentration, which has been modeling by both empirical and theoretical simulations perspectives. In the light J-V curve, which became soft at the T_{SUB} (640 ℃), it is indicated to cause the reduction of FF. From Figure 65 (right), the color J-V in different wavelength (460 to 700 nm) is revealed the theory

of voltage dependency in the carrier collection with a given wavelength and is relative to a lifetime. Thus, regarding T_{SUB} of 640 ℃, the V_{OC} &FF have been decreased shown in both Figure 65 (left) and Table 7.2, due to the passivation of absorber defect and diffusion length.

In summary, it is apparent that the impact of processing on the cell characteristics is suggested to attain the optimum Se composition, improve the grain structure of CST alloys, and increase p-type net doping concentration. The CST alloys can be formed in the ultimate uniform and homogeneous film in the first region of the absorber layer, where the junction of devices are potential to avoid to suffer the detrimental grain structure (void) in the interface via inter-diffusion bi-layer CdSe/CdTe process. The grain structure appears to grow larger with increasing the substrate temperature according to TEM cross-section images. Thus, it is also believed that the enhancement of grain size and grain boundary cloud be relative to increase the p-type net doping for improving the V_{OC}. The recent cell performance up to date is approximately 17.6 % for CST (x=20%)/CdTe device. The effect of Se compositions (x) on the performance of $CdSe_xTe_{1-x}$ films and photovoltaic devices fabricated by CSS using CST alloys sources have been investigated. The surface metrology and cross-section images showed that the high Se composition (x> 20%) of CST alloys films were increasing the grain growth and homogeneous layer of absorber stack layer with increasing T_{SUB} during the CSS deposition. Devices with high Se composition (x=25 %) exhibited improvement of net p-type doping in C-V measurement and minority carrier lifetime in the higher substrate temperature (620 ℃), which shown in the light and color J-V. No significant loss was observed in V_{OC} due to the lower CST bandgap (E_g=70 meV), considering that CdTe cells processed in a similar manner resulting in V_{OC} of 850 mV. Higher substrate temperatures appeared to promote CST/CdTe grain structure and higher doping concentration. An optimized fabrication process and extrinsic doping of CST can lead to both improvements in V_{OC} and J_{SC}.

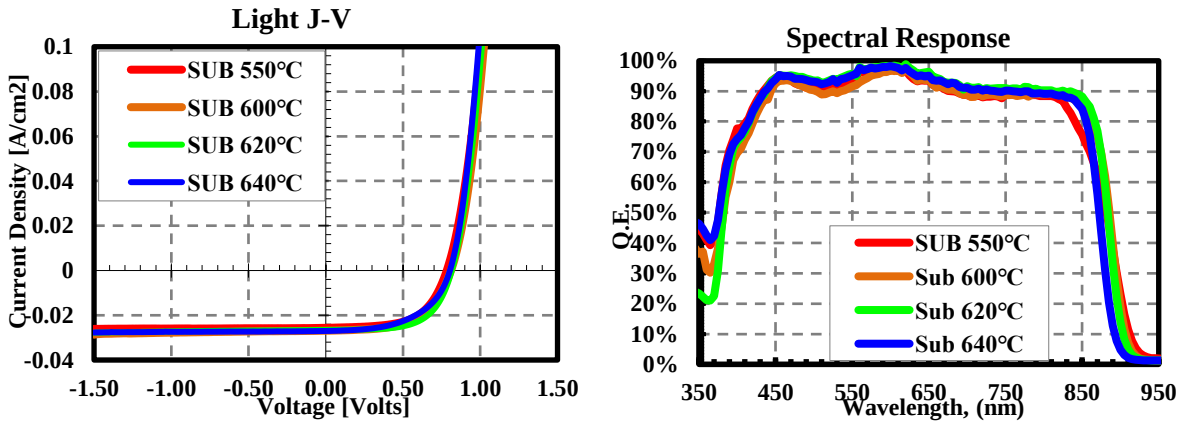


Figure 64 (left) Light JV and (right) SR for three devices fabricated with 1 µm thick CST alloys/ 3 µm thick CdTe and deposited at different substructure temperatures.

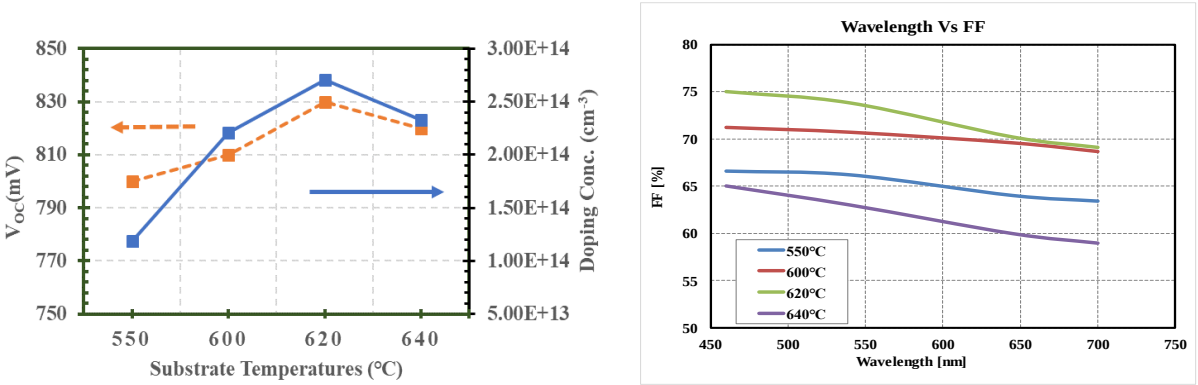


Figure 65 The (left) V_{OC} and doping concentration of CST (25% Se)/ CdTe devices in various T_{SUB} at He/O_2 ambient gas. The (right) color J-V (460 to 700 nm) for four devices fabricated with 1 µm thick CST alloys/ 3 µm thick CdTe and deposited at different substructure temperatures (550 to 640 °C).

7.6 Extrinsic Cu Doping on CST Devices

The effect of Cu doping in $CdSe_xTe_{1-x}$ (CST)/CdTe solar cells with varying amounts of Se (x) has been investigated. The Cu-based back contact was annealed at various temperatures in order to vary the amount of Cu in-diffusion. The solar cell configuration was ITO/MZO/CST/CdTe, where the composition of CST was varied from 5 to 20%. Net p-type doping was found to increase as the back-contact annealing temperature increased. All cells exhibited a decrease in V_{OC} with increased annealing temperature (i.e., higher Cu concertation), presumably due to a degradation of the lifetime with increased amounts of Cu. However, cells with

the highest Se composition appeared to exhibit a higher degree of tolerance to the amount of Cu – i.e., they exhibited a smaller loss in V_{OC} with the increased amount of Cu.

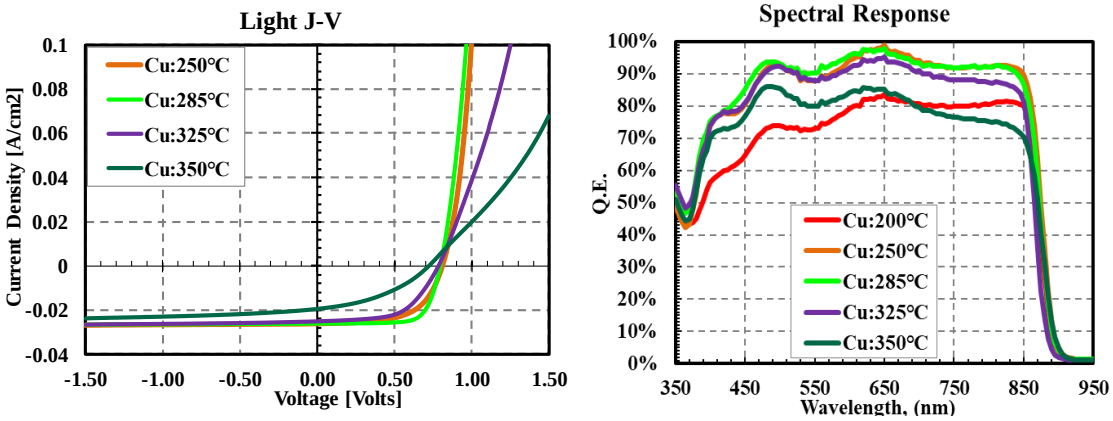


Figure 66 (left) J-V curve and (right) SR showed variation of Cu annealed temperatures (250 to 350 ℃) in Se 20% of CST alloy.

Today, the most essential challenge remains to increase the p-type net doping concentration of CST alloys and CdTe. The use of Cu for the formation of the back contact is also responsible for establishing the p-type doping and therefore plays a significant role in influencing both V_{OC} and FF. A certain amount of Cu is beneficial for CdTe solar cells performance. In contrast, excessive Cu-doped causes degradation in the performance of the cells as it forms lifetime-limiting defects. The back-contact annealing temperatures can be used to control the amount of Cu diffusing into a bulk material, and optimize performance.

Cu can typically form two types of defects in CdTe; a substitutional defect (Cu_{Cd}) and an interstitial defect (Cu_i). Cui is a shallow donor level (0.01 eV), and Cu_{Cd} is a deeper acceptor level (0.22 eV) [75]. The formation of Cu_{Cd} (following back contact processing) relies on the presence of Cd vacancies (V_{Cd}), which is a deeper acceptor than Cu_{Cd}. P-type doping levels achieved with Cu are in the range of ~10^{14} cm^{-3}, which has been sufficient to reach V_{OC}'s in the mid to high 800 mV range and yield low enough conductivity not to limit the FF of the cell.

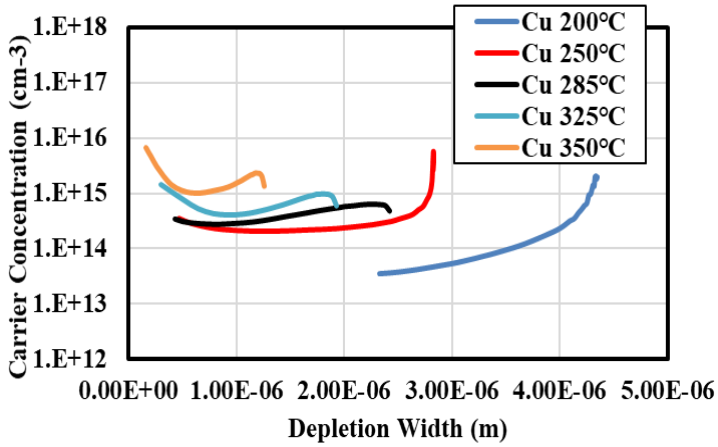


Figure 67 The doping concentration of CST (20% Se)/ CdTe devices in various Cu annealed temperatures (200 to 350 ℃) by C-V measurement.

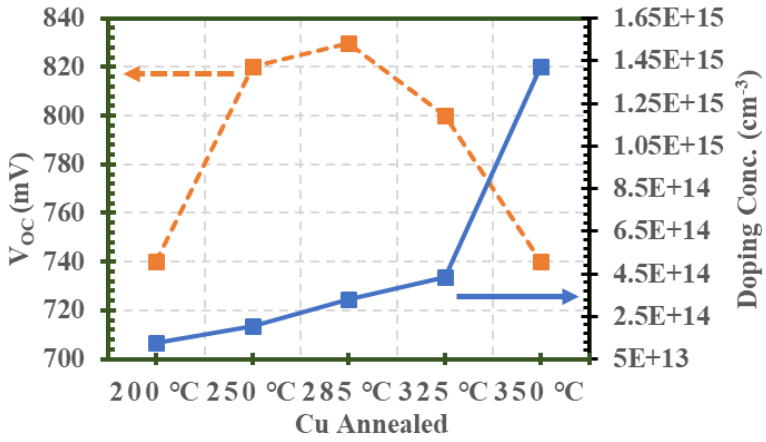


Figure 68 The V_{OC} and doping concentration of CST (20% Se)/ CdTe devices in various Cu annealed temperatures (200 to 350 ℃).

It is well known that the minority carrier lifetime is indispensable to improve the overall performance for CdTe thin film solar cells. In fact, the CdTe thin film solar cell has a relatively low tolerance for Cu due to a decrease in minority carrier lifetime, so that excessive Cu is detrimental for the CdTe cell. Alloying CdTe with CdSe has resulted in absorbers with significantly higher lifetimes.

Cu diffusion is a standard process for the formation of effective back contact and p-type net doping for CdTe solar cells. Recent advances in CdTe technology have demonstrated that the use of CST alloys as absorber layer can lead to substantially higher short circuit current (J_{SC}) and

efficiencies of 22 % have been demonstrated [122]. Therefore, investigating the p-type net doping concentration of CST is essential in order to understand the role of Cu in these alloys.

A set of CST solar cells (x=20 %) were processed @ different Cu annealing temperatures (200 to 350 ℃) in order to vary the amount of Cu incorporated into the absorber layer. Figure 66 (a) and (b) show the J-V and SR data, respectively. The results exhibit a trend similar to the traditional CdS/CdTe solar cells. The low Cu temperatures cause the rollover in the J-V, while the highest Cu annealing temperatures lead to excessive Cu doping and degradation in the minority carrier lifetime as shown at long wavelength behavior of the SR data. The optimal Cu temperature for the CST devices was found to be in the range of 285-290 ºC. This temperature is higher than what was found to be optimal for regular CdS/CdTe devices. The results may suggest that CST alloys can tolerate a higher Cu dose/doping than CdTe.

Carrier density as a function of distance from the bulk junction was extracted from room temperature capacitance-voltage (C-V) taken at 10 kHz. Figure 67 shows the doping concentration of CST (20% Se) devices processed at different Cu annealing temperatures (200 to 350 ℃) (same as samples in Figure 66.). The net doping concentration increases at higher annealing temperatures (i.e. higher amounts of Cu), which also results in smaller depletion width. At 350 ℃ the acceptor carrier concentration was approximately 1.45E+15 cm^{-3}. Figure 68 shows the V_{OC} and doping as a function of the Cu annealing temperature. V_{OC} reaches its maximum value @ 285 ℃, corresponding to a doping level of 4.00E+14 cm^{-3}. However, further increases in doping result in V_{OC} degradation due to an apparent lifetime degradation at these high Cu levels.

Figure 69 shows TRPL measurements for two samples annealed at 285 ℃ and 325 ℃ following the application of the Cu-back contact. The sample annealed at 285 ℃ exhibits a slower decay indicating a longer lifetime; the lifetime for that sample (annealed @ 325 ℃) is similar to

what was previously obtained for CdTe cells (i.e. without the CST alloy), while the sample annealed at 285 ℃ exhibits significantly higher lifetime (6-7X) and as shown in Table 6.2 higher efficiency.

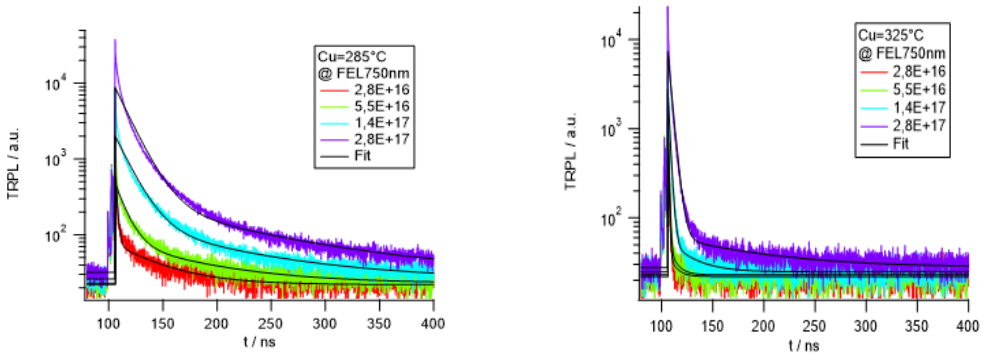


Figure 69 Time-resolved photoluminescence decay of the CST(20% Se)/CdTe devices in various excitation power at Cu annealed temperature 285 and 325 ℃ respectively.

Solar cells annealed at low temperatures (< 250℃) exhibit high current density and relatively high fill factor, but low and inconsistent V_{OC} typically in the range of 750 – 800 mV; although lifetime data is not available at this time for samples annealed @ 200 ℃, the low V_{OC} can be attributed to the lower doping (see Figure 65 above) and potentially lower lifetimes. Solar cells annealed at the highest temperatures (350 ℃) exhibited the highest net doping; however, their V_{OC} was lower than samples annealed @ temperatures in the range 250 – 285 ℃; this is believed to be due to significantly lower lifetimes assuming the trend shown in Table 7.3 continues.

Table 7.4 The minority carrier lifetime and cell efficiency of CST/CdTe devices in different Cu annealed temperatures.

Cu annealed temperatures (℃)	**Estimated Minority carrier lifetime (ns)**	**Cell efficiency (%)**
285	95	17.5%
325	15	13.5%

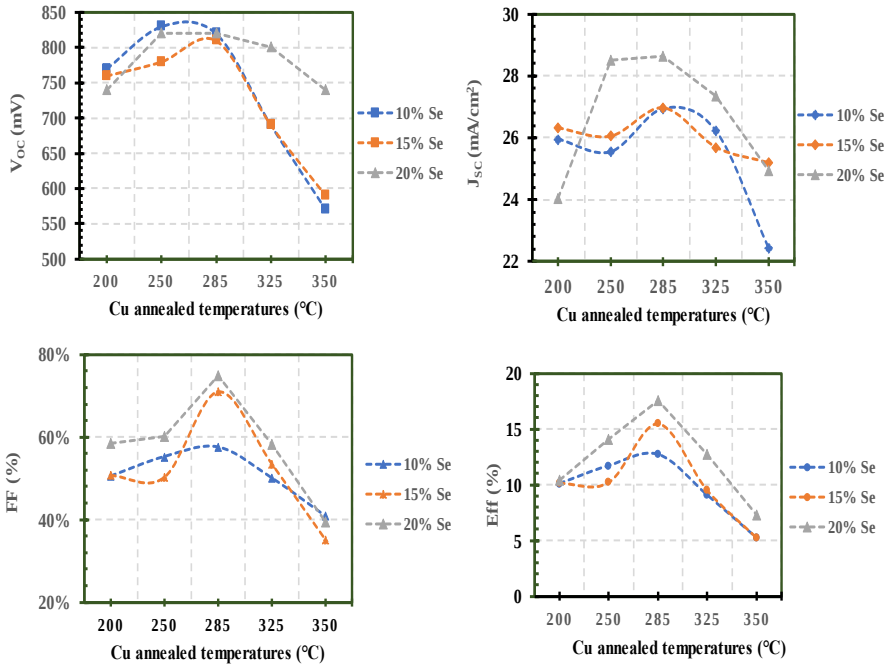


Figure 70 The solar cell parameters (V_{OC}, J_{SC}, FF, and Eff) in various Se compositions (x=10, 15, and 20 %) of CST alloy at different Cu annealed temperatures (250 to 350 °C).

Similar experiments as those described in Figure 66 (left) and (right) were repeated for smaller Se compositions (x=10 & 15 %). The device results for all compositions are summarized in Figure 70. The overall trends are similar for all compositions. Optimum performance is achieved around 285 to 290 °C, while higher temperatures lead to performance degradation. However, the decrease in V_{OC} for the devices with x=20 % (highest Se composition used to-date) is significantly smaller, suggesting that the addition of Se may allow a higher amount of Cu to be incorporated in the CST/CdTe cells. The best performance achieved to-date as a result of optimizing Se composition and Cu annealing temperatures was achieved for x=20 % and T_{ANN}=290 °C (for Cu); this cell (not the same as in Table 7.4) had a V_{OC}, J_{SC}, and FF of 820 mV, 28.6 mA/cm^2, and 74.8 % respectively, corresponding to an efficiency of 17.6 % (without AR coating) (Figure 70).

Cu back-contact is used as a way to extrinsically dope CdTe, and it is crucial for the performance of CST/CdTe solar cells. The net p-type concentration for CST appears to decrease

as the Se composition increases, which along with the resulting lower bandgap lead to lower V_{OC}. This work studied CST allows with Se composition up to x=20 %. The effect of Cu doping was found to be similar to what is known about CdTe cells (i.e.no CST): an optimum amount of Cu must be achieved to maximize doping and lifetime, with excessive Cu doping leading to performance degradation due to lifetime degradation. The amount of net p-doping can be controlled by varying the back-contact annealing temperatures (200 to 350 ℃) to adjust the amount of Cu in-diffusion. It is found out the optimum for solar cell performance at annealing temperature range is 285 to 290 ℃, which is higher than the optimum temperature used for CdTe cells (i.e., no CST). It was also shown that the minority carrier lifetime significantly improves (6-7X) in CST alloys and that the decrease in V_{OC} at high levels (i.e. excessive) of Cu is smaller at high Se compositions. This suggests that CST compounds can potentially tolerate more Cu than CdTe.

7.7 Extrinsic Group V Doping on CST Devices

The extrinsic doping with group V materials is widely used in the polycrystalline CdTe thin film solar cells. Typical group V p-type dopants include Phosphorus, Arsenic, and Antimony. Group V elements generally replace Te (Group VI materials) to form acceptor states. According to CdTe summary of defects, P and As produce shallow acceptor defects (0.07 and 0.1 eV from VBM respectively); thus the CST alloys are suggested to result in similar defect states with typical CdTe [123]. Unlikely the Group I dopants (Cu), interstitials were not found to be the primary compensating defects for group V materials in CST alloys. When a P or As atom try to occupy a Te site, it generates the substitutional defect P_{Te} or As_{Te} where it is surrounded by four Cd atoms [124]. The challenge of using Group V dopants is the high formation energy to form P_i and As_i in the compensation defects. In this case, the CST alloy has remained unknown process for Group V p-type doping in the defect states compared to CdTe. Also, under equilibrium growth conditions,

the Femi level was found be located at 0.32eV and 0.36eV for P-doping elements by using P and As respectively [125]. The devices have corresponded to a net acceptor density of above 10^{14} cm^3. In the following section, As were incorporated in CST and CdTe. The effect of the group V dopants was investigated and compared to undoped CST/CdTe cells. Incorporating these elements and sequentially activating them to form the desired acceptors can be challenging. Dopants can be introduced through post-growth incorporation methods using diffusion, which may require very high temperatures to achieve sufficient concentrations in bulk. [126].

Initially, the study of $CdCl_2$ HT has been investigated on the low As doped CST samples. In Table 7.5, the As-deposited sample shows the lower performance due to the lack of Cl doping and lifetime issue. The $CdCl_2$ HT temperatures start to increase the V_{OC} improve considerably as same as the current density, which shows in Figure 71. The SR is demonstrated that the lifetime increased the carrier collection as the $CdCl_2$ HT temperatures increased. However, the low As doped sample in the best $CdCl_2$ temperature at 430°C does not show any sign of enhancement. Even though the C-V measurement reveals the doping concentration is increased from 2E+14 to 8E +14 cm^{-3}, but those likely are the effect from the Cl doping to bring up the doping concentration which is shown in Figure 72. Thus, the next study is relative to various doping levels of As on CST and doped CdTe. The summary table is displayed in Table 7.6. As doping levels are initially increasing that is contributed to increased V_{OC} due to the p-type net doping improve shown in Figure 73. The C-V measurement shows the higher As doped CST on the devices leads to increase the doping concentration up to 1E+15 cm^{-3}. As a matter of fact, the highest amount of As doped sample reveals the reduction of FF and $J_{SC,}$ which is believed to be the loss of over doping due to decreased depletion width and lifetime in Figure 74. Therefore, it is crucial to find an optimum As doping level for increasing the V_{OC} without reduction of overall performance. The highest V_{OC} is

demonstrated up to 850 mV with ungraded As-doped CST/CdTe devices. Finally, in Table 7.7, the summary of the devices fabrication process in various compound materials and paraments show the essential to improve the cell efficiency to fulfill the achievement. The promising device configuration is ITO/MZO/As-doped CST/doped CdTe, which has the highest V_{OC} and p-type net doping concentration for further improvement in future work.

Table 7.5 The performance of devices with low As doped CST in various $CdCl_2$ HT.

	V_{OC} (mV)	FF (%)	J_{SC} (mA/cm^2)	Efficiency (%)
As deposited	600	49.90%	20.41	6.11
$CdCl_2$ 410°C	760	50.70%	26.32	10.14
$CdCl_2$ 430°C	820	65.30%	29.57	15.87
$CdCl_2$ 440°C	810	52.90%	27.14	11.52

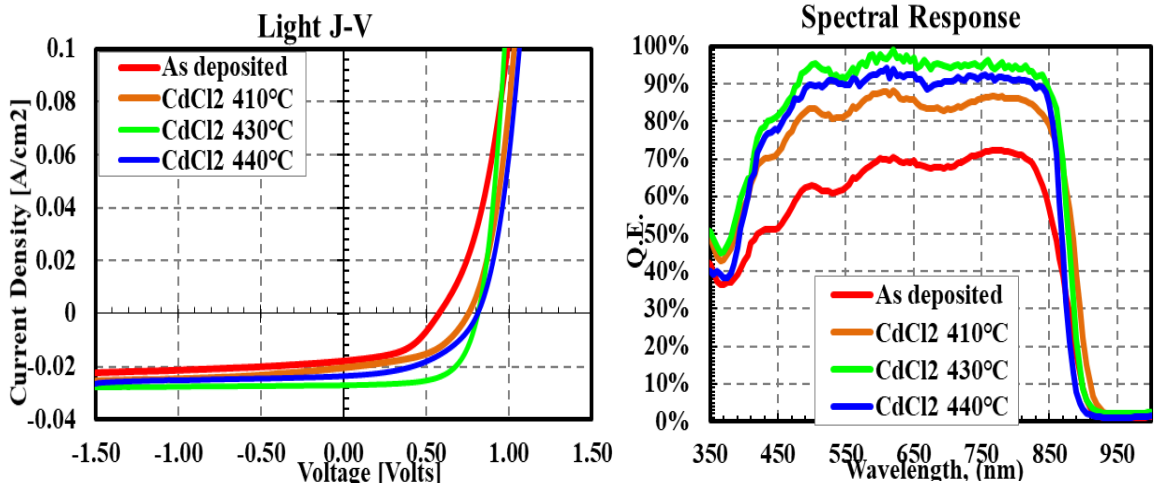


Figure 71 The (left) light J-V and (right) SR of low As doped CST (20% Se) devices in as-deposited and various $CdCl_2$ HT temperatures (410 to 440 °C).

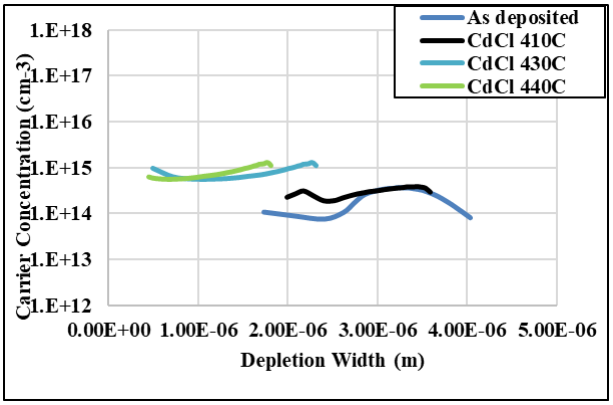


Figure 72 The doping concentration of low As doped CST (20% Se) devices in as-deposited and various $CdCl_2$ HT temperatures (410 to 440 ℃) by C-V measurement.

Table 7.6 The performance of devices with different As doping levels and undoped CST.

$CdCl_2$ HT 430℃	Voc (mV)	FF (%)	Jsc (mA/cm^2)	Efficiency (%)
Undoped CST	830	65.60%	28.85	15.71
Low As doped CST	840	66.90%	29.32	16.48
Medium As doped CST	850	59.80%	27.56	14.01
High As doped CST	810	38.40%	26.54	8.26

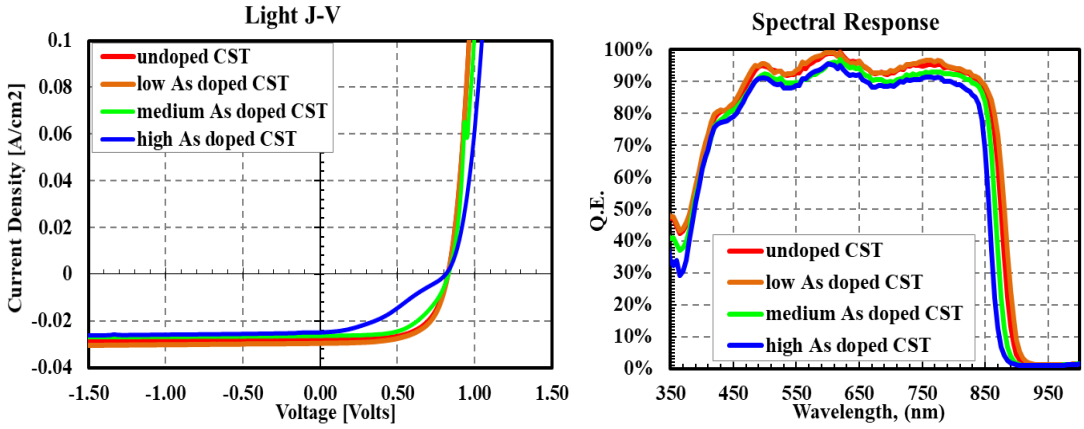


Figure 73 The (left) light J-V and (right) SR of in various As doping levels on CST (20% Se) and doped CdTe on the devices.

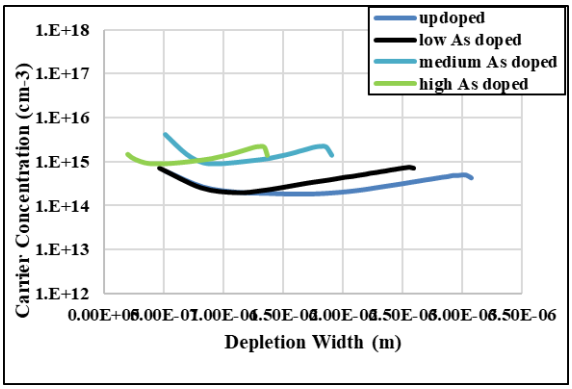


Figure 74 The doping concentration in various As doping levels on CST (20% Se) and doped CdTe on the devices by C-V measurement.

Table 7.7 The performance summary of devices for various type of fabrication processes.

CdTe			$CdSe_xTe_{1-x}$/CdTe		
Parameter	CdS	$Mg_yZn_{1-y}O$	Extrinsic doping		CSS
			Undoped	Doping	
V_{OC} (mV)	**830-850**	860	**810**	**850**	800
J_{SC} (mA/cm²)	**24.5**	26.5	**28.5**	**29.3**	27.2
Carrier Conc. (cm^{-3})	**8.77E+14**	2.23E+14	**1.75E+15**	**5.72E+15**	1E14

$CdSe_xTe_{1-x}$ (x=20%)

CHAPTER 8

CONCLUSION

The impact of MZO as a window layer in CdTe cells has been investigated. Several MZO characteristics were studied; the effect of its thickness, composition, and the impact of annealing. It was found that the composition of MZO affects the position of its conduction band and that a composition that results in a positive ΔEc (*"a small spike"*) is beneficial to the cell performance. It was also found that MZO/CdTe devices are relatively more tolerant than the traditional CdS/CdTe device to the $CdCl_2$ heat treatment, as optimum annealing temperatures exceeded the typical 400℃ used for CdS/CdTe. The MZO/CdTe junctions could be annealed at temperatures as high as 430 ℃ without delamination or flaking. It was also found that the MZO/CdTe interface must be annealed in the presence of CdS vapors at temperatures over 600 ℃ in order to avoid the formation of a junction that results in the rollover in the cell's JV characteristics. The instability of the MZO/CdTe interface will be continuously investigated in future research.

The process of forming and depositing CST films and MZO/CST/CdTe junctions was also investigated. Inter-diffusion of CdSe is one of the methods to form the CST layer as an absorber; thus the effect of CdSe thickness on the Se profile in CST films produced by annealing CdTe/CdSe bilayers has been investigated. TEM analysis suggested that CST films synthesized with "thin" (< 300 Å) CdSe films resulted in well inter-diffused CST films and a homogeneous grain structure. Thick (>300 Å) CdSe films resulted in CST alloys with smaller grain structure at the interface and inhomogeneous Se profiles, with a Se-rich region and Te-rich region. These findings can be used to support the loss in V_{OC} for devices fabricated with CST films synthesized via annealing of

CdTe/CdS bilayers, and suggest that interdiffusion of CdSe/CdTe bilayers is only viable for small Se compositions in order to avoid void formation due to the *"Kirkendall effect ."*

The effect of Se composition on MZO/CST/CdTe devices has also been studied using direct sublimation of CST alloys using the CSS process. Devices with higher Se composition exhibited higher current density and minority carrier lifetime. However, lower V_{OC} (750 – 800 mV) still was measured in devices with high Se composition of CST alloys that it can be attributed to low doping concentration, reduction of bandgap, and small grain size in the absorber layer. The CSS substrate temperature and the $CdCl_2$ annealing temperatures have been found to be critical in achieving high-quality grain structures, with grains that extend throughout the absorber thickness. As substrate temperature is increased from 550 ℃ to 620 ℃, the grain size increases by a factor of 3X, and grains can extend through the entire thickness of the absorber. The V_{OC} has improved from 800 to 830mV in devices with Se composition (> 20%). Also, devices annealed at 430 ℃ for $CdCl_2$ HT exhibited a graded Se profile vs. an abrupt profile for lower temperatures, suggesting that the $CdCl_2$ HT can be used to adjust the Se profile in the CST films.

Cu-based back-contacts are critical to the performance of CST/CdTe solar cells. P-type net doping in CST decreases as the Se composition increase and can result in lower V_{OC}. For this work, the effect of Cu on CST films with 20% Se composition has been investigated; the back contact annealing temperature was used to vary the amount of Cu diffused into the absorber. An optimum amount of Cu can optimize the acceptor net doping concentration for optimum V_{OC} and FF. However, excessive Cu doping seems to be detrimental to performance due to lifetime degradation. It was found out the best temperature for annealing the Cu based back contacts was in the range 285 to 290℃, and above or below this temperature, the V_{OC} decreased. This

temperature range is higher than what is typically used for USF CdTe (only) cells. It is therefore suggested that CST films can potentially tolerate more Cu than CdTe.

Finally, arsenic (As) was used to dope CST and CdTe films during the CSS. A doping level of 10^{16} cm^{-3} was achieved with a corresponding V_{OC} of 850 mV for a Se composition of 20%. This V_{OC} is higher than what has been achieved for undoped CST/CdTe junctions in this work.

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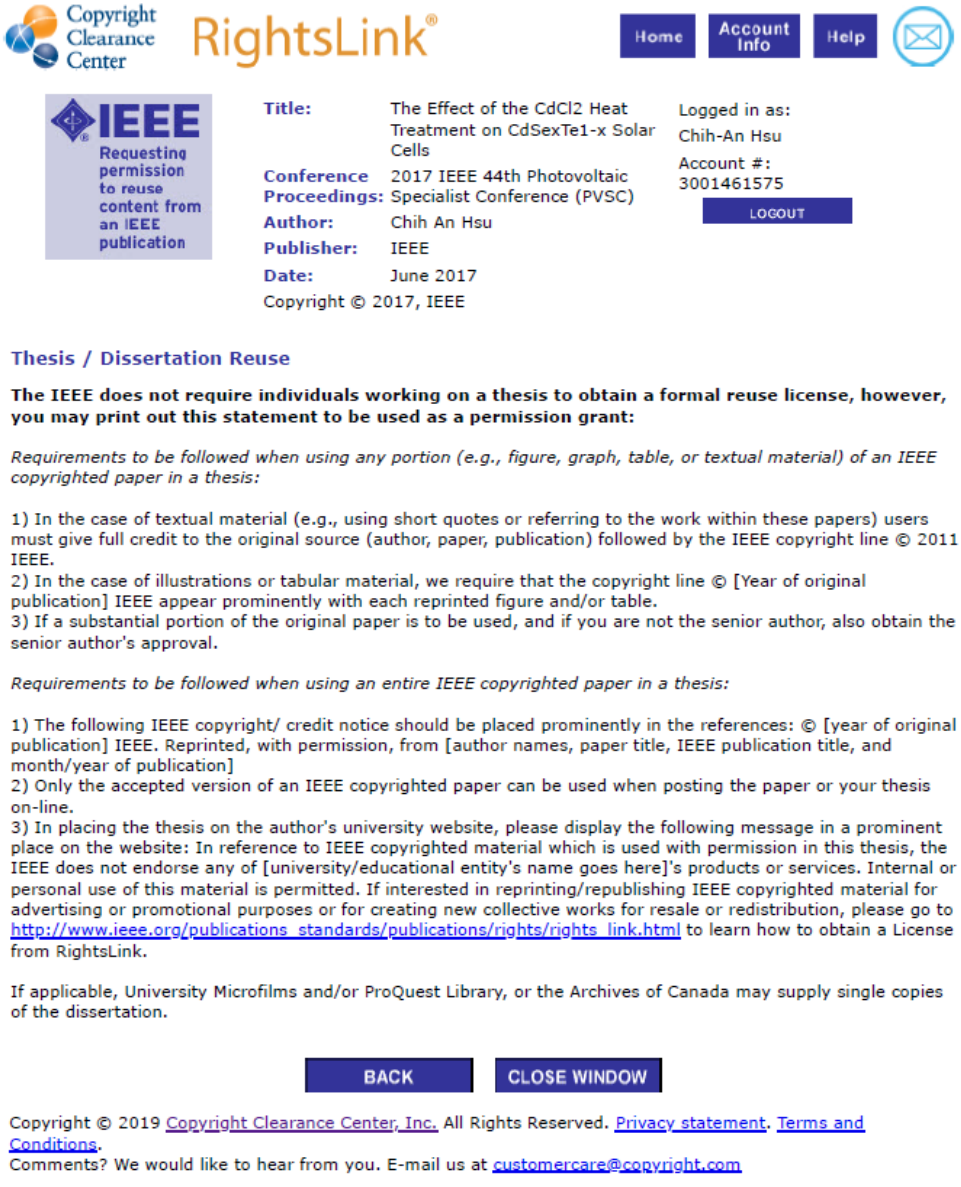

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